ELECTRICAL MODELING, DESIGN AND CHARACTERIZATION OF TAPERED THROUGH-PACKAGE-VIAS IN GLASS INTERPOSERS FOR HIGH-PERFORMANCE APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

Jialing Tong

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2016

ELECTRICAL MODELING, DESIGN AND CHARACTERIZATION OF TAPERED THROUGH-PACKAGE-VIAS IN GLASS INTERPOSERS FOR HIGH-PERFORMANCE APPLICATIONS

Approved by:

Dr. Rao R. Tummala, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Suresh K. Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Andrew F Peterson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Venkatesh Sundaram
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: August 8, 2016

To God, my parents, sisters, and friends.

ACKNOWLEDGEMENTS

First, I would like to express my deepest gratitude to my advisor, Prof. Rao R Tummala, for giving me a unique opportunity to join the 3D Systems Packaging Research Center (PRC) at Georgia Tech. He has been constantly directing and shaping my thesis. In addition, he has been very supportive of my research ideas. His passion and readiness to learn new technologies will continue to inspire me. I am proud and grateful to be his student.

I am also very grateful to my committee members: Dr. Andrew F Peterson, Dr. Oliver Brand, Dr. Suresh Sitaraman, and Dr. Venkatesh Sundaram for their time and valuable feedback to improve my thesis. The way they look at problems have made a profound impact on my way of thinking. Further, I wish to thank Dr. Venkatesh Sundaram for mentoring me daily since I joined PRC at Georgia Tech.

I feel blessed to be able to work with such a knowledgeable team at PRC. My special and genuine thanks go to Dr. Raj Pulugurtha, Dr. Vanessa Smet, Dr. Kadappan Panayappan, Dr. Fuhan Liu, Dr. Himani Sharma, Prof. Wolter, and Dr. Melinda Varga for their willingness to discuss and help me whenever I run into troubles. Next, I want to thank the PRC staff: Karen May, Patricia Allen, Brian McGlade, Chris White, and Jason Bishop, as they are always there for me. Finally, I want to thank all of the visiting engineers for their unconditional support: Yoichiro Sato (AGC), Tomonori Ogawa (AGC), Toshitake Seki (NGK-NTK), Yutaka Takagi (NGK-NTK), Hiroyuki Matsuura (NGK-NTK), Makoto Kobayashi (Namics), Satomi Kawamoto (Namics), Taiji Sakai (Fujitsu), Akira Mieno (Atotech), and Ryuta Furuya (Ushio).

My stay at PRC would not have been as good without the support of my colleagues: Koushik Ramachandran, Vijay Sukumaran, Dibyajat Mishra, Gokul Kumar, Srikrishna Sitaraman, Saumya Gandhi, Parthasarathy Chakraborthy, Gary Menezes, Chinmay Honrao, Bhupender Singh Chauhan, Qiao Chen, Xian Qin, William Vis, Sangbeom Cho, Bruce Chou, Kaya Demir, Hao Lu, Yuya Suzuki, Timothy Huang, Brett Sawyer, Scott McCann, Min Suk Kim, Nathan Huang, Zihan Wu, Chandrashekaran Nair, Ninad Sahane, Vidya Jayaram, Atomu Watanabe, Teng Sun, Tailong Shi, Rui Zhang, Haksun Lee, Chintan Buch, Shreya Dwarakanath, Sukhadha Viswanathan, Karan Bhangaonkar, Srisurya Yadavalli, and Mehul Mehra. And thanks to my friends, living in Atlanta was one of the most joyful experiences. I will never forget those happy days with them.

Lastly, I owe my sincerest gratitude to my family. My parents have been making every effort to love and support me. Wherever I go and whatever I do, they are always with me. I also want to extend my deep appreciation to my sisters and their husbands, as they always step up whenever I need them. I am extremely grateful for their love and support.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

C	Capacitance
C_g	Series capacitance of microstrip gap
C_{GLS} or C'_{GLS}	Capacitance of glass
C_m	Mutual capacitance
d	Microstrip feed line length
δ_s	Skin depth
D	Via diameter
D_{pad}	Pad diameter
ε_0	Vacuum permittivity
ε_{eff}	Effective dielectric constant
ε_r	Relative permittivity of glass
$\varepsilon_{r,\,k}$	Relative permittivity of dielectric
g	Capacitive microstrip gap width
γ	Propagation constant
G	Conductance
G_{GLS} or G'_{GLS}	Conductance of glass
Γ	Reflection coefficient
h	Substrate thickness
h_{RMS}	Average value of surface roughness
$\vec{J}_S$	Surface current density
k_p	Proximity factor
K_C	Capacitive coupling coefficient
K_H	Hammerstad coefficient

K_L	Inductive coupling coefficient
l	1/4 of the ring circumference
l_p	CPW pad length
λ	Wavelength
L	Inductance
L_m	Mutual inductance
L_{TPV}	Parasitic via loop inductance
μ_0	Vacuum permeability
μ_r	Relative permeability of glass
N	Number of slices
ω	Angular frequency
p	Center-to-center via pitch
φ	Angle between signal and two return TPVs
r_x	Radius of via at vertical position x
ρ	Resistivity of the copper
R	Resistance
R_{TPV}	Parasitic via resistance
$\tan \delta$	Loss tangent of glass
t_{cu}	Copper thickness of pads
θ	Via taper angle
t_m	Conformally-plated copper thickness
T	Polymer thickness
W	Microstrip line width
x	Vertical position
x_0	vertical position at which radius is equal to skin depth

x_a	Signal conductor position of CPW pad
x_b	Gap position of CPW pad
x_c	Ground conductor position of CPW pad
Y_v	Input admittance of one TPV
Z_0	Characteristic impedance of microstrip ring resonator
Z_s	Reference impedance
Z_{in}	Input impedance

LIST OF ABBREVIATIONS

2.5D	Two-and-a-half-dimensional
3D	Three dimensional
A2V1	Two aggressors and one victim
A4V1	Four aggressors and one victim
AFM	Atomic-force microscopy
ArF	Argon fluoride
AR	Aspect ratio
CTE	Coefficient of thermal expansion
CO_2	Carbon dioxide
CPW	Coplanar waveguide
DRIE	Deep reactive-ion etch
Cu	Copper
EM	Electromagnetic
EMI	Electromagnetic interference
FEXT	Far-end crosstalk
FPGA	Field-programmable gate array
G4S1	Four ground TPVs with one signal TPV
G6S1	Six ground TPVs with one signal TPV
GaAs	Gallium arsenide
GS	Ground-signal
GSG	Ground-signal-ground
HFSS	High frequency structural simulator
IC	Integrated circuit

ITRS	International Technology Roadmap for Semiconductors
LNA	Low-noise amplifier
NEXT	Near-end crosstalk
PDN	Power distribution network
PEC	Perfect electrical conductor
PWB	Printed wiring board
RDL	Redistribution layer
RF	Radio frequency
SAP	Semi-additive process
SEM	Scanning electron microscope
Si	Silicon
SOLT	Short-Open-Load-Through
SOP	System-on-package
TDR	Time-domain reflectometry
TEM	Transverse electromagnetic
TiSa	Titanium sapphire
TiW	Titanium tungsten
TSV	Through-silicon via
TPV	Through-package via
VNA	Vector network analyzer
VNI	Visual Network Index
WLP	Wafer-level packaging

SUMMARY

Three dimensional (3D) packaging technologies are being developed to address the escalating demand for data traffic at lowest power consumption, smallest form factors, and lowest cost. Glass has been proposed as a compelling alternative to silicon and the best packaging substrate for interposer, high-performance, and millimeter-wave applications. Through-package vias (TPVs) are a critical building block, particularly in 3D architectures to interconnect ICs assembled on both sides of the glass. Typically, TPVs have a tapered shape as a result of high speed laser ablation and other commonly used via formation methods. Until now, the effects of taper on the electrical performance of TPVs in glass have yet to be reported.

The objectives of this research were to model, design, and characterize tapered TPVs in glass interposers to provide design guidelines for TPVs by quantifying their impact on electrical performance. To achieve these objectives, three research tasks were carried out: 1) electrical modeling of TPVs by taking into account both geometric and material effects; 2) design of TPVs for minimum impedance discontinuity and crosstalk; 3) millimeter-wave characterization of TPVs to extract via parasitics.

A wideband scalable circuit model was proposed to model tapered TPVs in glass, with analytical or semi-analytical equations derived for the *RLCG* parameters. The proposed model was then verified against full-wave simulations and measurements. Based on this model, the effects of the via taper and TPV processes including copper plating, via sidewall roughness, polymer liners, and nonlinearly tapered shapes were analyzed in terms of electrical parameters.

The design of tapered TPVs in glass interposers was studied for improved signal integrity in terms of signal transition, impedance discontinuity, and crosstalk. The first task was to study the *S*-parameters and the time-domain eye diagrams of TPVs with various taper angles. The second task was to analyze the TPV-induced impedance discontinuity using time-domain reflectometry. Design techniques were proposed and demonstrated to minimize such impedance discontinuity. Finally, the basic Ground-Signal-Ground TPV crosstalk structures were modeled by an equivalent circuit that was verified against full-wave simulations and measurements, and five techniques were proposed and studied to suppress the crosstalk noise.

The electrical parasitics associated with TPVs in glass were experimentally characterized up to 50 GHz using two different methods, namely a short-circuit method and a ring-resonator method. An equivalent circuit including via parasitics was proposed to analyze the short-circuit method, and a transmission-line-based equivalent network was proposed to analyze the ring-resonator method. In addition, the sensitivity of each method with respect to via resistance and inductance was studied. Based on these two methods, test vehicles were designed and fabricated using a panel-scalable double-sided metallization process. The resistance and inductance of a single via were extracted from the measurements for each method.

CHAPTER 1

INTRODUCTION

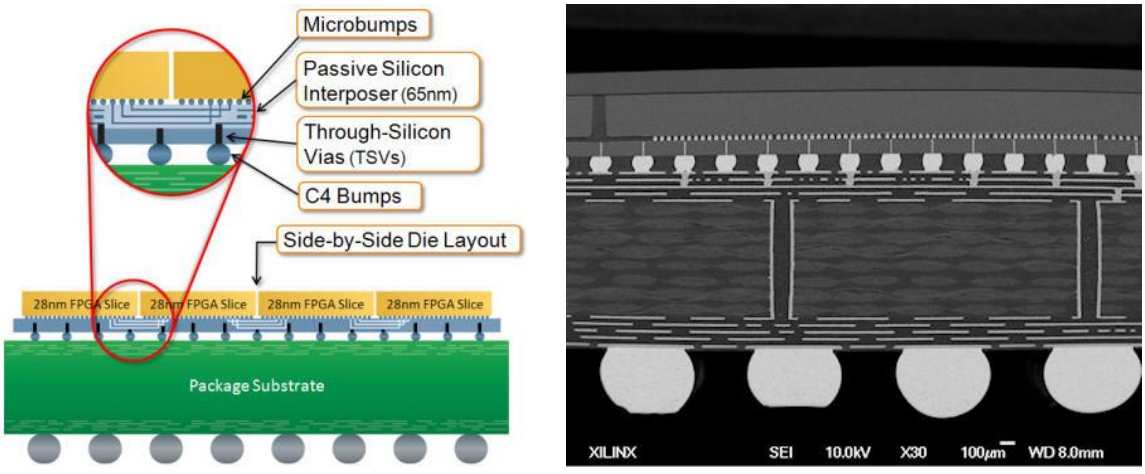
Cloud computing provides users and enterprises with Internet-based capabilities to store and process gargantuan data in the data centers with high computing power and low cost of service. Further, wireless communication enables global mobility and ubiquitous connectivity to any device through wireless networks. Both cloud computing and wireless communication have been driving the demand for high computing capability, fast transmission speed, and increased functionality and bandwidth. The International Technology Roadmap for Semiconductors (ITRS) projects that by 2020, the data rate on the package-level will increase to 55 Gbps with on-chip frequency of 12.36 GHz, and the maximum package pin count will reach 7902 in high-performance applications for cloud computing [1]. In addition, the Cisco Visual Network Index (VNI) report forecasts that the overall mobile data traffic in wireless communication will rise to 30.6 exabytes per month by 2020, with the average mobile network connection speed increased by more than threefold to 6.5 Mbps and the average data traffic from smartphones reaching 4.4 GB per month [2]. To accomplish some of these, millimeter-wave frequencies, such as 28 GHz and 38 GHz [3], have been proposed as one of the disruptive approaches to increase the bandwidth of next generation wireless communication systems.

1.1 The Rise of Glass Packaging

To address the escalating demand for more and faster data traffic at lower power consumption, smallest form factor and lowest cost, transistor scaling following Moore's law has been the singular approach at chip level for the past decades. However, it is becoming apparent that transistor scaling is slowing down, taking longer time from node

to node than previous transitions, because of the growing cost and complexity of transistor scaling, as well as the dielectric leakage in the fronts and the RC delays in the back ends [4]. Hence, there is no longer a cost reduction as the next node is introduced with higher transistor density.

More-than-Moore technologies were subsequently pursued to achieve further system miniaturization at lower cost. One of the approaches is to reduce the interconnection length by 3D stacking of integrated circuits (ICs), which has been successfully applied to stacking of memory ICs. Another architecture is 2.5D side-by-side chip integration at close proximity, enabled by ultrahigh I/O density interposers with much smaller bump pitch than the traditional flip chip packages. Both 3D stacking and 2.5D integration have been on the silicon substrate. For instance, silicon interposers were first demonstrated by Xilinx in late October 2010 for high-performance 28 Gbps field-programmable gate array (FPGA) systems [5]. The schematic cross section of this novel architecture is shown in Figure 1.1 (a), while an actual cross-section image of the Xilinx 28-nm Virtex-7 device is presented in Figure 1.1 (b), created by a scanning electron microscope (SEM).



(a) (b)

Figure 1.1: (a) Schematic cross-section view of the Xilinx's silicon interposer technology, and (b) SEM cross-section of the 28-nm Xilinx's Virtex-7 device [6].

However, silicon interposers with through-silicon vias (TSVs) face a set of challenges, including the complex manufacturing processes, the limited wafer size, and most importantly the notoriously high substrate loss associated with silicon that hinders the maximum data rate per channel. Figure 1.2 shows the measured time-domain eye diagram for a 4 mm channel with TSVs in silicon interposers [7]. It can be seen that the eye diagram is closed at 10 Gbps. Hence, equalization techniques are needed to open the eye diagram, which increases the cost due to the additional equalizer design and fabrication.

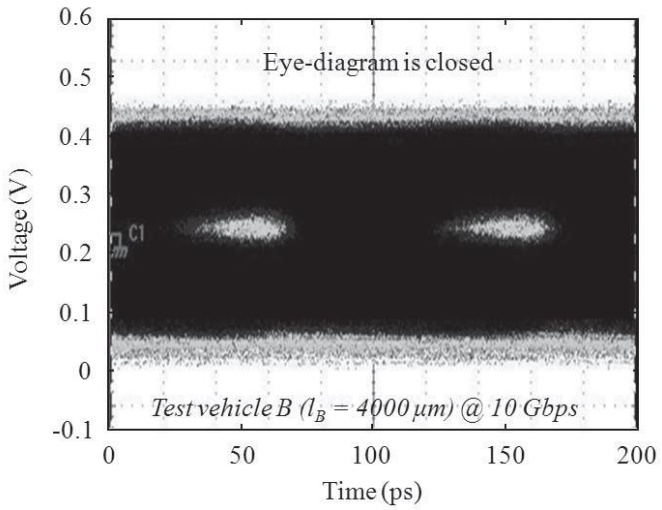


Figure 1.2: Measured eye diagram for a 4 mm channel with TSVs in silicon interposers at 10 Gbps [7].

3D glass interposers, proposed and demonstrated by the 3D Systems Packaging Research Center (PRC) at Georgia Institute of Technology (GT), with double side IC assembly interconnected by ultra-short and ultra-fine pitch through-package vias (TPVs) in 30-100um thin glass interposers, offer a more scalable and potentially lower cost solution [8]. Such 3D glass interposers have been developed as part of the vision of system-on-package (SOP), illustrated in Figure 1.3, to integrate the entire system on a

single substrate by system scaling of active and passive components to achieve highest performance at lowest power and cost [9, 10].

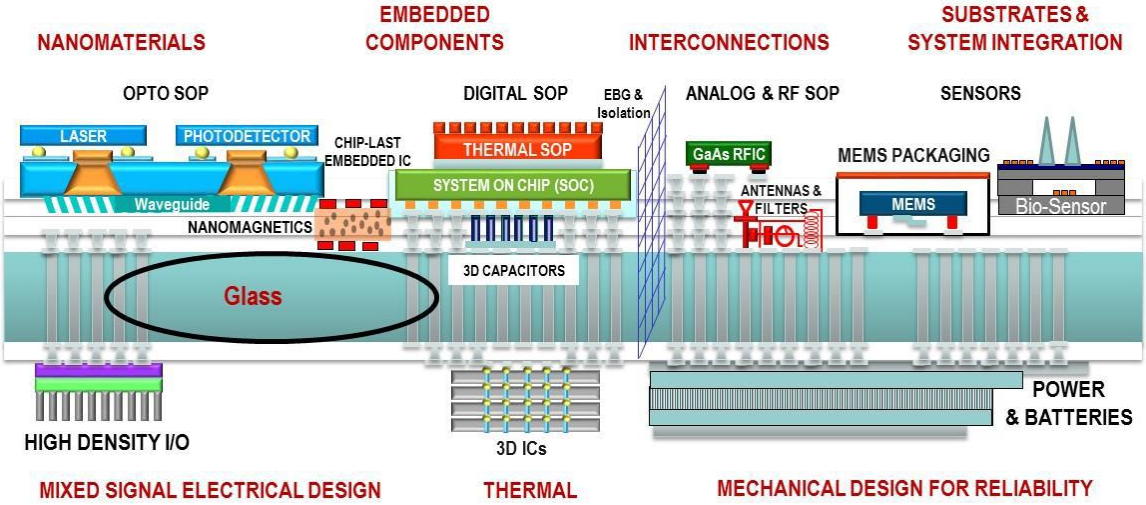


Figure 1.3: Conceptual view of system-on-package (SOP) with through-package vias (TPVs) in glass interposers (Prof. Rao Tummala).

Glass substrates have emerged as a promising candidate for system scaling, due to their:

- Excellent electrical properties for certain glass, including low dielectric constant (ε_r or Dk ≈ 5.3) and ultra-low loss tangent (tanδ or Df = 0.006 at 10 GHz) [11]
- Tailorable coefficient of thermal expansion (CTE) from 3 to 9.8 ppm/K, enabling a close CTE match with any type of die, such as silicon (Si, 2.6 ppm/K) or gallium arsenide (GaAs, 6.86 ppm/K), and possibility to assembly the glass directly on board even at large package size
- Smooth surface (< 1 nm) for least conductor loss and fine-feature lithography [12]
- Zero water absorption in harsh environments
- Superior dimensional stability
- Panel-based processability and high-throughput via formation for low cost [13, 14].

1.2 Through-Package Vias in Glass Interposers

Through-package vias (TPVs) are a critical building block, particularly in 3D architectures to interconnect ICs assembled on both sides of ultra-thin interposers. As illustrated in Figure 1.4, TPVs support two primary functions, (1) power delivery from the printed wiring board (PWB) to the ICs, and (2) high-speed or high frequency signal transition. In an ideal case, TPVs are expected to have the following electrical metrics:

- Parasitic resistance = 0 Ω, resulting in no DC IR drop
- Parasitic inductance = 0 pH, resulting in no simultaneous switching noises
- Characteristic impedance = 50 Ω for impedance match
- Insertion loss = 0 dB for maximum transmission
- Crosstalk = 0, resulting in no noise generation.

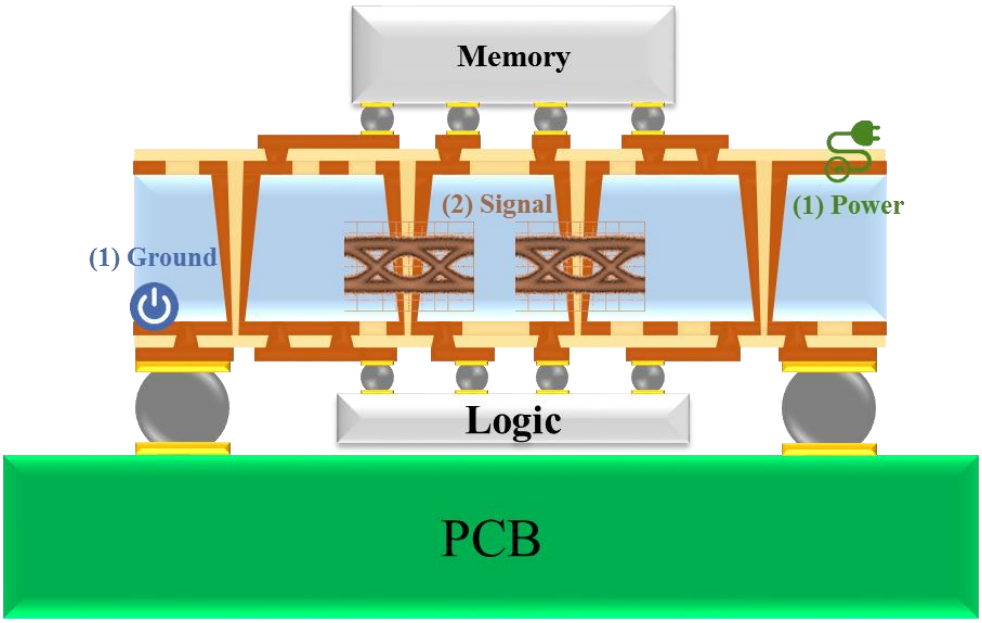


Figure 1.4: Schematic cross-section showing two functions of TPVs: (1) power delivery and (2) signal transition.

While there has been a large amount of published research to understand those metrics of TSVs in silicon, which will be discussed in detailed in CHAPTER 2, the work on TPVs in glass is preliminary [15-17]. Further, TPVs in glass differ from TSVs in two

ways, as highlighted in Table 1.1. First, there are three types of fundamental electromagnetic (EM) modes, namely skin-effect mode, slow-wave mode, and quasi-TEM (transverse electromagnetic) mode, which exist in TSVs depending on the resistivity of the silicon and the operation frequency [18, 19], whereas only one TEM or quasi-TEM mode exists in glass TPVs, as shown in Figure 1.5. This is because glass, as an excellent insulator, has much higher resistivity than silicon, a semiconductor material. Second, TSVs formed by the deep reactive-ion etch (DRIE) have 90° vertical profiles [20-22], as shown in Figure 1.6, while TPVs in glass formed by laser ablation have a tapered shape with taper angles no larger than 88°.

Table 1.1: Comparison between TPVs in glass and TSVs in silicon

Characteristic		**TPVs in Glass**	**TSVs in Silicon**
EM Mode		Frequency-independent	Frequency-dependent
Via Shape	Process	Laser ablation	Deep reactive-ion etching
	Geometric parameters	≤ 88°	90°

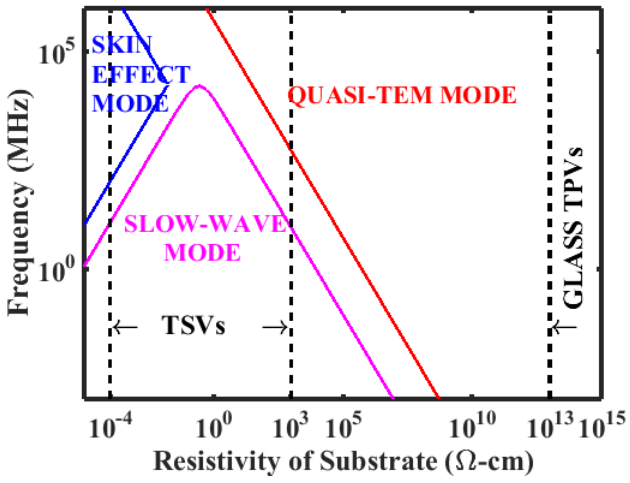


Figure 1.5: Resistivity-frequency domain chart showing TSVs in silicon and TPVs in glass.

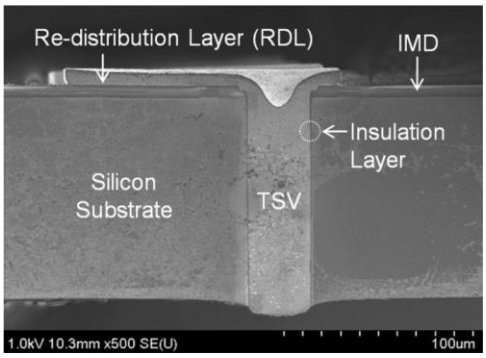


Figure 1.6: SEM image of a TSV fabricated by the deep reactive-ion etching [23].

Table 1.2 summarizes the current TPV formation methods in glass. The taper angle of TPVs can vary from as low as 75^o, typical of a TiSa laser formation [24], to as high as 88^o, for a focused electrical discharge micro-machining [25].

Table 1.2: TPV formation methods and the taper

Process	**TiSa Laser**	**ArF Excimer Laser**	**CO_2 Laser**	**Photo-Sensitive**	**Electrical Discharge**	**Laser Induced Etching**	**Corning**
Top Φ	277 μm	50 μm	120 μm	66 μm	60 μm	20 μm	53 μm
Bot Φ	75 μm	20 μm	50 μm	35 μm	40 μm	15 μm	47 μm
THK	500 μm	180 μm	500 μm	250 μm	300 μm	80 μm	110 μm
Taper	78.58^o	85.24^o	86.00^o	86.45^o	88.09^o	88.21^o	88.44^o

The TPV formation technology resulting in the lowest 78.58^o taper angle, as shown in Figure 1.7, is the titanium-sapphire (TiSa) laser. The argon fluoride (ArF) excimer laser and the carbon dioxide (CO_2) laser can form TPVs with taper angles of about 86^o [26], as well as the patterning process with photo-sensitive glasses [24], with the cross-section view of TPVs formed by these three process depicted in Figure 1.8. There are three methods that can form TPVs of about 88^o taper angles, namely the

focused electrical discharge method in Figure 1.9 (a) [25], the laser induced etching method in Figure 1.9 (b) [27], and the Corning's drilling method in Figure 1.9 (c) [13]. Currently, 88^{o} is the steepest taper angle reported in the literature.

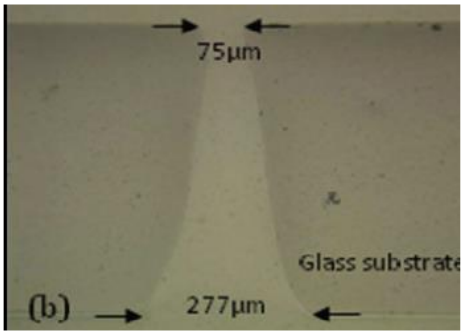
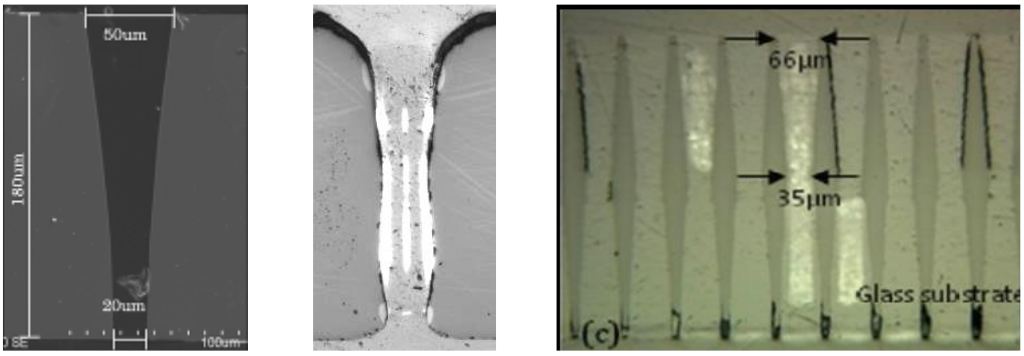
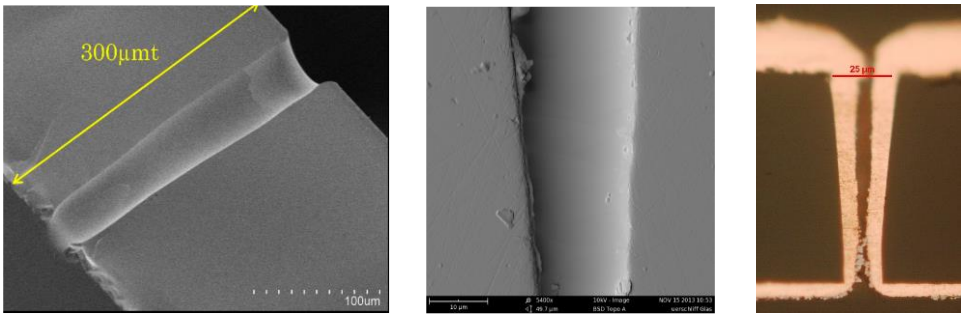


Figure 1.7: Optical image of TPV formed by the TiSa laser [24].



(a) (b) (c)

Figure 1.8: Optical image of TPV formed by (a) the ArF excimer laser [28], (b) the CO_2 laser [26], and (c) the patterning process on a photo-sensitive glass [24].



(a) (b) (c)

Figure 1.9: Optical image of TPV drilled by (a) the focused electrical discharge method [25], (b) the laser induced etching method [27], and (c) the Corning's drilling method [13].

The variance in geometric parameters of TPVs, such as taper angle, sidewall roughness, and polymer liners, introduces a number of fundamental challenges in electrical modeling, design, and characterization of TPVs, which forms the basis of this thesis research.

1.3 Research Objectives

The objectives of this research are to model, design, and characterize tapered TPVs in glass to provide design guidelines to meet the needs of emerging high computing and wireless communication systems. Three specific goals were defined in this research:

1) Fundamentally study the effect of via geometric parameters including taper, sidewall roughness, and polymer liners on the electrical parameters for glass interposers

2) Optimize the TPV design for maximum transmission and minimum noises, leading to a set of design guidelines for TPVs in glass

3) Experimentally measure via parasitics accurately.

Table 1.3 summarizes the critical electrical metrics associated with the research objectives of this dissertation beyond prior arts on TSVs in silicon and TPVs in glass.

Table 1.3: Research objective beyond prior art

Metrics	Prior Art		Goals
	TSVs	TPVs	
Resistance (Ω @ GHz)	0.105 @ 2	missing	< 1 @ 50
Inductance (pH @ GHz)	262.5 @ 2	missing	< 200 @ 10
Z_0 discontinuity (Ω)	18%	10%	5%
Insertion loss (dB @ GHz)	3.20 @ 20	0.197 @ 20	0.15 @ 20
Crosstalk (dB)	<-15	<-20	<-30
Maximum freq. (GHz)	50	40	50

1.4 Technical Challenges and Research Tasks

To achieve these goals, the following research challenges are identified in electrical modeling, design, and characterization, as shown in the schematic cross-section of Figure 1.10 and summarized in Table 1.4.

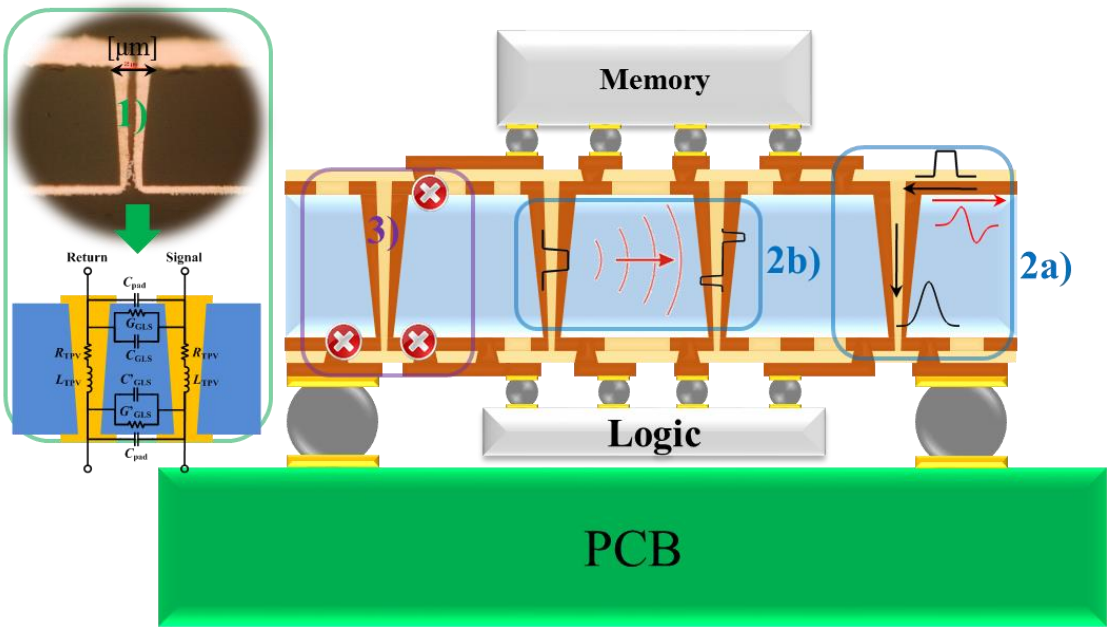


Figure 1.10: Schematic cross-section with modeling challenges labeled as 1), design challenges labeled as 2a) and 2b), and characterization challenges labeled as 3).

Table 1.4: Technical challenges and research tasks

	Challenges	Tasks
Modeling	1a. Accuracy 1b. Computational efficiency	Electrical modeling of tapered TPVs
Design	2a. Impedance discontinuity 2b. Crosstalk	Design of tapered TPVs for improved signal integrity
Characterization	3a. Accuracy & Wideband 3b. De-embedding	Millimeter-wave characterization of tapered TPVs

Modeling: It requires a high accuracy to precisely capture the effects of via taper in micrometer regime. In addition to the accuracy, a typical interposer size is about 16

mm × 16 mm for a single die packaging and 35 mm × 25 mm for a two-die packaging, and the number of TPVs in such a package will be in the order of 10^3. It takes a significant amount of time to simulate the entire interposer with TPVs using 3D commercial electromagnetic (EM) solvers during the design cycle. Computational efficiency is exacerbated by non-uniform mesh sizes in 3D EM solvers for the tapered shape, as tapered TPVs have a conical shape with the bottom diameter smaller than the top diameter which in turn needs a mix of fine and coarse meshes to capture the difference of the tapered shape, as shown in Figure 1.11. Thus, the accuracy and the computational efficiency are the main challenges in modeling tapered TPVs.

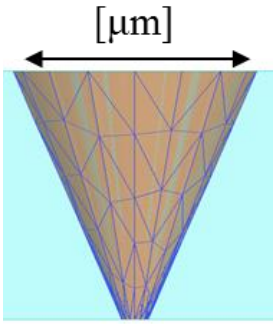


Figure 1.11: Tetrahedron meshes of conical TPVs in glass interposers.

Design: As the high-frequency voltage or current signals propagate till the end of redistribution layer (RDL) and are about to transit through TPVs, they see an impedance discontinuity from the junction between RDL and TPVs, as shown in Figure 1.12. Such an impedance discontinuity generates reflections, resulting in time-domain signal degeneration. Furthermore, because TPVs are placed in close proximity to each other at fine pitch, the crosstalk from aggressor TPV to victim TPV might cause unintentional transistor switching, leading to bit errors. Therefore, impedance discontinuity and crosstalk are identified as the technical challenges in design of tapered TPVs.

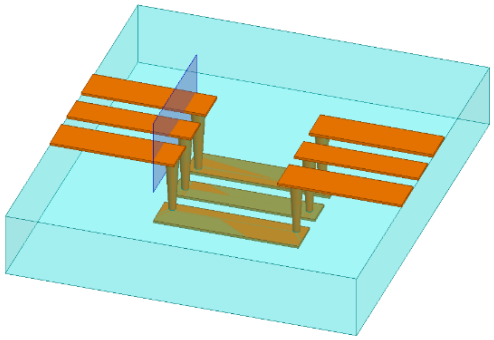
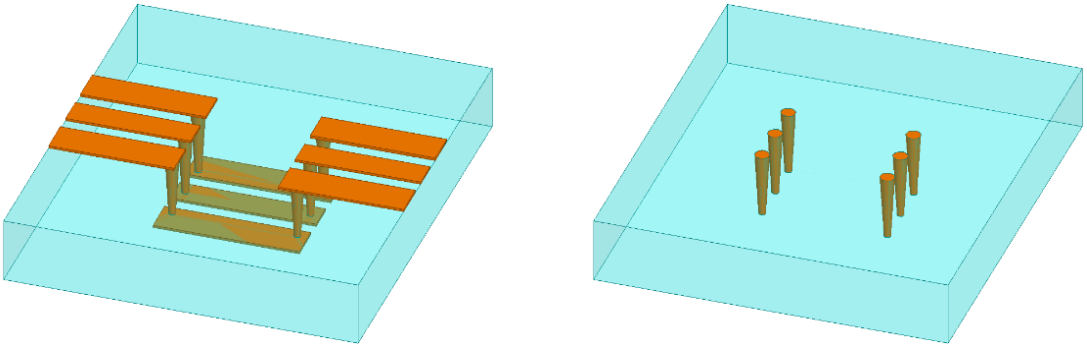


Figure 1.12: Impedance discontinuity between RDL and TPV.

Characterization: Given the micrometer-sized TPVs and the wide bandwidth requirements for high computing and wireless applications, accurate experimental characterization is required to extract the TPV parasitics to shorten design cycles. Even though a double-sided probing system can directly access the top and bottom sides of the TPVs [29], it is important to enable the use of coplanar probe systems and de-embed the effect of RDL as indicated in Figure 1.13, as most of the measurement facilities are setup for coplanar circuit probing. In summary, the accurate wideband measurement and de-embedding of the RDL effect are the two main challenges identified in the experimental characterization of tapered TPVs.



(a) (b)

Figure 1.13: Demonstration of de-embedding (a) line-via chains to (b) via only.

To address the aforementioned challenges, three main research tasks are proposed and summarized in Table 1.4.

Modeling: To improve the computational efficiency with high accuracy, a physics-based wideband circuit model is required to model tapered TPVs in glass, while also accounting for geometry and material effects. It is also necessary to verify the proposed circuit model against the 3D EM simulations and the measurements. Further, the taper effect and the process effects on each circuit element in the proposed model need to be investigated.

Design: The effect of taper on signal transition through TPVs is necessary. Then, the impedance discontinuity needs to be analyzed through the TDR simulations to understand its relation to the taper. In addition, the crosstalk between TPVs needs to be studied to determine the coupling mechanisms with various taper angles. Based on the study, design techniques should conclude how to minimize the impedance discontinuity and crosstalk.

Characterization: Novel characterization approaches are required for accurate wideband measurement of TPV parasitics with the RDL de-embedded. Fundamental derivation and sensitivity analysis of these novel characterization approaches are desirable to understand the underlying principles. Finally, based on these novel approaches, test vehicles will be designed, fabricated and measured to extract TPV parasitics.

1.5 Thesis Organization

This dissertation is organized into six chapters as follows:

CHAPTER 1 describes the strategic need and the research objectives of this work. The technical challenges and the proposed research tasks are identified to achieve these objectives.

CHAPTER 2 summarizes the prior art in electrical modeling, design and characterization of TSVs in silicon interposers and TPVs in glass interposers.

CHAPTER 3 describes in detail a proposed wideband scalable circuit model for tapered TPVs in glass interposers. The computation scheme for the *RLCG* elements in this model is also presented with analytical expression for resistance (*R*) and semi-analytical expressions for inductance (*L*), capacitance (*C*), and conductance (*G*). Then, this model is verified against 3D EM simulations and measurements in terms of *S*-parameters, and the convergence and sensitivity studies are conducted. Finally, the effects of the via taper and via processes are comprehensively studied in terms of the *RLCG* parameters.

CHAPTER 4 discusses the design of tapered TPVs in glass interposers for improved signal integrity. The signal transition through tapered TPVs is first studied in terms of *S*-parameters and eye diagrams. Then, the impedance discontinuity of tapered TPVs is analyzed through TDR simulations, and two design techniques are proposed to minimize this impedance discontinuity. Finally, the crosstalk of TPVs is studied for various taper angles, and two of the worst-cases scenarios are evaluated in the time domain. Five design techniques are proposed and compared to suppress the crosstalk.

CHAPTER 5 presents two novel characterization methods for TPVs in glass interposers, namely the short-circuit method and the ring-resonator method. Equivalent circuit model is proposed for each method, and the sensitivity are derived to understand the fundamental principles. Also, test vehicles are designed and fabricated by a novel low-cost, panel-based process to metallize high-aspect-ratio TPVs. Finally, the TPV parasitics are extracted from the measured *S*-parameters based on the proposed two methods.

CHAPTER 6 summarizes the key findings and scientific contributions of this dissertation. It also summarizes the design guidelines for tapered TPVs in glass interposer s to achieve highest performance. This chapter also identifies future work in this area.

CHAPTER 2

LITERATURE SURVEY

CHAPTER 1 introduced the focus of this research on the electrical modeling, design, and characterization of TPVs in glass interposers having a tapered shape ($\leq 88^{o}$), considerably different from TSVs in silicon interposers having a cylindrical shape ($\approx 90^{o}$). The fundamental challenges identified to achieve the objectives are: 1) the accuracy and the computational efficiency for precise via modeling; 2) the impedance discontinuity and the crosstalk induced by TPVs for design; 3) the accurate wideband measurement of TPVs with RDL de-embedding. This chapter provides a comprehensive review of the published literature related to the technical challenges organized into electrical modeling, design, and characterization of both TSVs in silicon and TPVs in glass.

2.1 Prior Art on Via Modeling

This section reviews the most-cited research work on TSVs in silicon and the limited work on TPVs in glass.

2.1.1 TSVs in Silicon

Extensive research work has been completed in the past to model TSVs as a lumped circuit with equations derived for each component in the circuit. Essentially, all these modeling work can be classified into four groups: 1) circuit modeling with closed-form expressions for *RLCG*; 2) modeling of MOS capacitance in TSVs to improve the accuracy; 3) full-wave modeling using advanced computational EM techniques to improve the computational efficiency; 4) modeling of tapered TSVs.

1). Prof. Joungho Kim's research group at KAIST in South Korea proposed a high frequency equivalent circuit model for TSVs in 2005 [30] and 2006 [31]. The parameters

in the circuit model were extracted from the measurement of *S*-parameters using a vector network analyzer (VNA) up to 20 GHz. In 2011, a high-frequency scalable electrical model was proposed including not only the TSV, but also the bump and the redistribution layer (RDL) [23]. The scalability of these models was verified by simulations using a 3D field solvers with parametric variations, while their validity was experimentally confirmed by the frequency-domain and time-domain measurements. Prof. Eby G. Friedman and his team [32] from University of Rochester have provided closed-form expressions of the resistance, capacitance, and inductance for TSVs in 2009. The closed-form expressions account for the TSV length, diameter, dielectric thickness, and spacing to ground. 3D numerical simulations were also used to verify the proposed model, revealing a good agreement between simulation and the physical models with the maximum error less than 8%.

2). Later, Katti [33] from IMEC of Belgium, Xu [34] from University of California, Santa Barbara and Bandyopadhyay [35] from PRC at Georgia Institute of Technology individually solved the 1D Poisson's equation for the MOS capacitance using TSV geometry parameters, the doping concentration, and the depletion region in their circuit models. Katti verified the computation of the MOS capacitance by C-V measurement; Xu verified the proposed TSV model by using full-wave simulations, while Bandyopadhyay verified the proposed model through the measurement of the power distribution network (PDN).

3). Some other research projects were conducted for full-wave modeling of TSVs. Han [36] from Georgia Institute of Technology proposed an efficient method to compute the equivalent network parameters of TSVs by solving Maxwell's equations in integral form. This method used a small number of global modal basis functions and was expected to be much faster than discretization-based integral-equation methods. Liu [37] from Agency for Science, Technology, and Research in Singapore used another method based on the magneto-quasi-static theory with a Fourier–Bessel expansion approach.

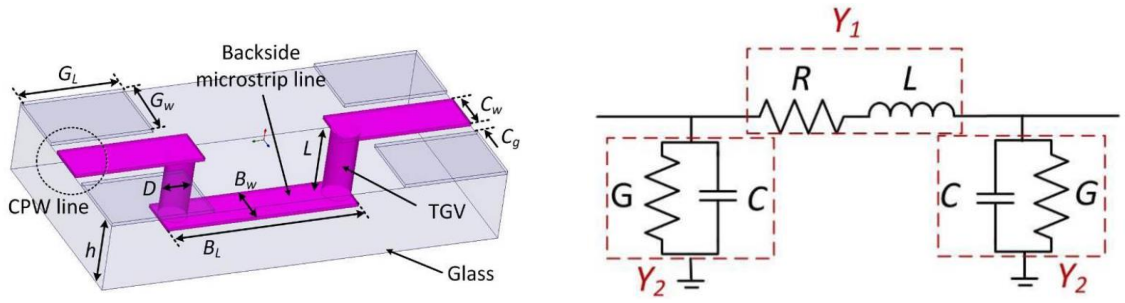
Rigorous closed-form formulas for the resistance and inductance of TSVs were derived, whereas analytical formulas from static solutions were used to compute the capacitance and conductance. This method captures the important parasitic effects of TSVs, including the skin effect, proximity effect, lossy effect of silicon, and semiconductor effect. Cheng [38] from National Taiwan University proposed a novel macro-π model based on the conformal mapping technique for a low pitch-to-diameter ratio TSV pair. The proposed *CG* model rigorously considered the proximity effect, and closed-form formulas were derived for a given TPV geometry. Through comparison with 3D full-wave simulations, the accuracy and the efficiency of these three methods were validated.

4). Some laser TSV formation methods yield a tapered shape instead of a cylindrical shape. Hence, Liang [39] from Shenzhen Institutes of Advanced Technology in China developed closed-form expressions to calculate the parasitic resistance and inductance of tapered TSVs, with maximum errors of 2% and 5% at low frequency for the resistance and the inductance, respectively, when compared to results from EM simulations. Xie [40] from Georgia Institute of Technology proposed and verified a hybrid approach based on conical modal basis functions combined with the cylindrical TSV modeling method for tapered TSVs. Liu [41] from Nanjing University of Science and Technology in China evaluated the capacitance and conductance of TSVs using the moment method, considering the multilayer media along the vertical direction and different shapes. It was found that the capacitance of tapered TSVs decreased with the increase in the slope angle and the pitch, which was beneficial in reducing the propagation delay.

2.1.2 TPVs in Glass

While there are many studies on electrical modeling of TSVs in silicon, the literature on modeling of TPVs in glass is limited, especially on understanding the effects of process induced geometric and material variations on the electrical performance.

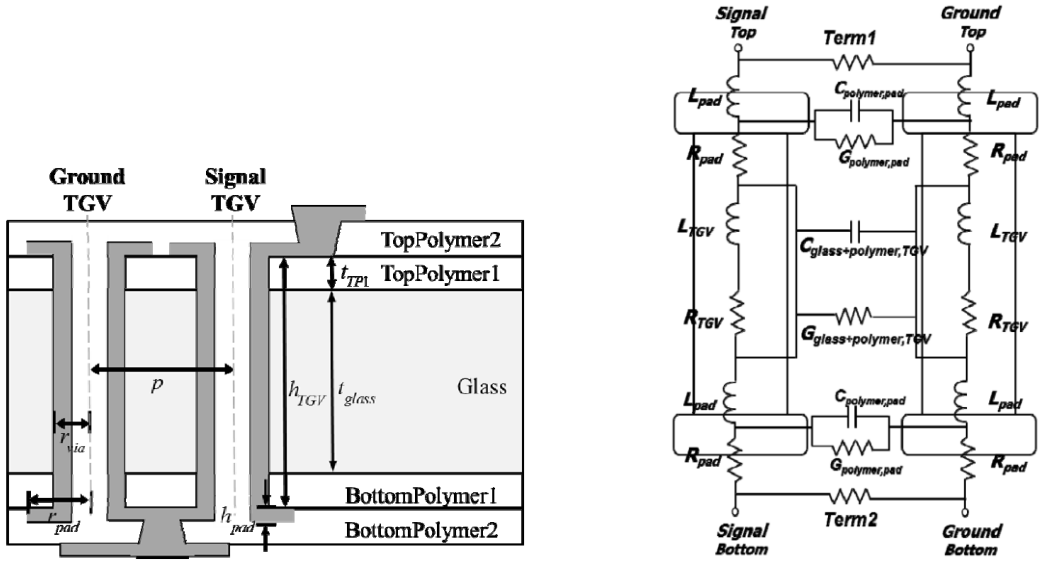
Kim [42] from University of Florida modeled TPVs in glass substrates shown in Figure 2.1 (a), as an equivalent π-circuit model in Figure 2.1 (b), and the lumped element parameters (*RLGC*) were extracted from 3D EM simulations. It was pointed out that the TPV with a diameter of 90 μm and a height of 500 μm, buried in a glass substrate with ε_r = 7.9 and tanδ = 0.008, had a resistance of 2.2 Ω, an inductance of 0.3 nH, a conductance of 0.01 S, and a capacitance of 1.8 pF at 1 GHz.



(a) (b)

Figure 2.1: (a) Perspective view of the dual-via chain structure, and (b) equivalent π-circuit model.

Kim [43] from KAIST of South Korea proposed a precise *RLGC* circuit model, as shown in Figure 2.2 (b), for single-ended TPVs in glass, as shown in Figure 2.2 (a), and expressions were provided for *RLGC* as a function of design parameters such as TPV height, diameter and pitch, and material properties. Then, the proposed model was verified up to 40GHz with full-wave simulations, and the electrical characteristic of TPVs in glass was analyzed by the proposed model. However, the model was based on the assumption of cylindrical vias, and the authors mentioned the worthiness of modifying the model for tapered vias.



(a) (b)

Figure 2.2: (a) Cross-section view of TPVs in glass interposers, and (b) electrical circuit model with *RLGC* components.

Therefore, it can be seen that a wideband scalable circuit model for tapered TPVs in glass interposers is still missing. And, a comprehensive study on the effects of taper and process-induced variation has yet to be reported in glass interposers.

2.2 Prior Art on Via Design

This section provides a brief overview of selective publications on via design for TSVs in silicon and TPVs in glass.

2.2.1 TSVs in Silicon

Due to the semi-conductive nature of silicon substrates, the noise coupling, i.e. crosstalk, between TSVs is a major concern for TSV design.

Xu [44] from Rensselaer Polytechnic Institute investigated the crosstalk noise of TSVs during high-speed operations though simulations in the frequency and time domains. A few guidelines were provided to decrease the crosstalk: (a) the fast rising

time devices should be avoided unless required by the performance; (b) enlarging the TSV pitch and shortening the TSV height reduce the crosstalk noise; (c) a high-resistivity substrate is preferred. In another paper of Xu's [45], it was pointed out that the rise time had little degradation when a signal propagated along the TSV, and the Z_{load} curve suggested TSV capacitive characteristics. The TSV radius should be optimized, and tapered TSVs are preferred in terms of electrical performance. The coaxial TSV was also examined [46], concluding that coaxial TSVs are superior to other TSVs in electrical performance due to the smaller time constants and frequency-dependent dynamic power.

Cho [47] from KAIST in South Korea proposed a noise-isolation technique using a guard ring. The proposed technique was experimentally demonstrated for noise isolation between the TSV and substrate contact, yielding a noise isolation of -17 dB at 100 MHz and -10 dB at 1 GHz.

From these published articles, it can be seen that one of the main concerns for TSV design is to reduce the crosstalk arising from the losses in the silicon substrate.

2.2.2 TPVs in Glass

Chien [48] from Industrial Technology Research Institute in Taiwan studied the TPV array shown in Figure 2.3 (b) that is constituted by six ground TPVs with one signal TPV (G6S1). This study involved simulations and measurements in the frequency range of 0.1 - 20 GHz. It was concluded that without ground planes or signal pads, the G6S1 array had identical characteristics with coaxial TPV in Figure 2.3 (a), and when ground planes and signal pads were added, as shown in Figure 2.3 (c), the extracted *RLGC* values of TPVs increased and the characteristic impedance Z_0 decreased. Finally, the authors reported that the meshed ground in Figure 2.3 (d) would not significantly change the electrical characteristics of G6S1 array compared to a solid ground below 20GHz.

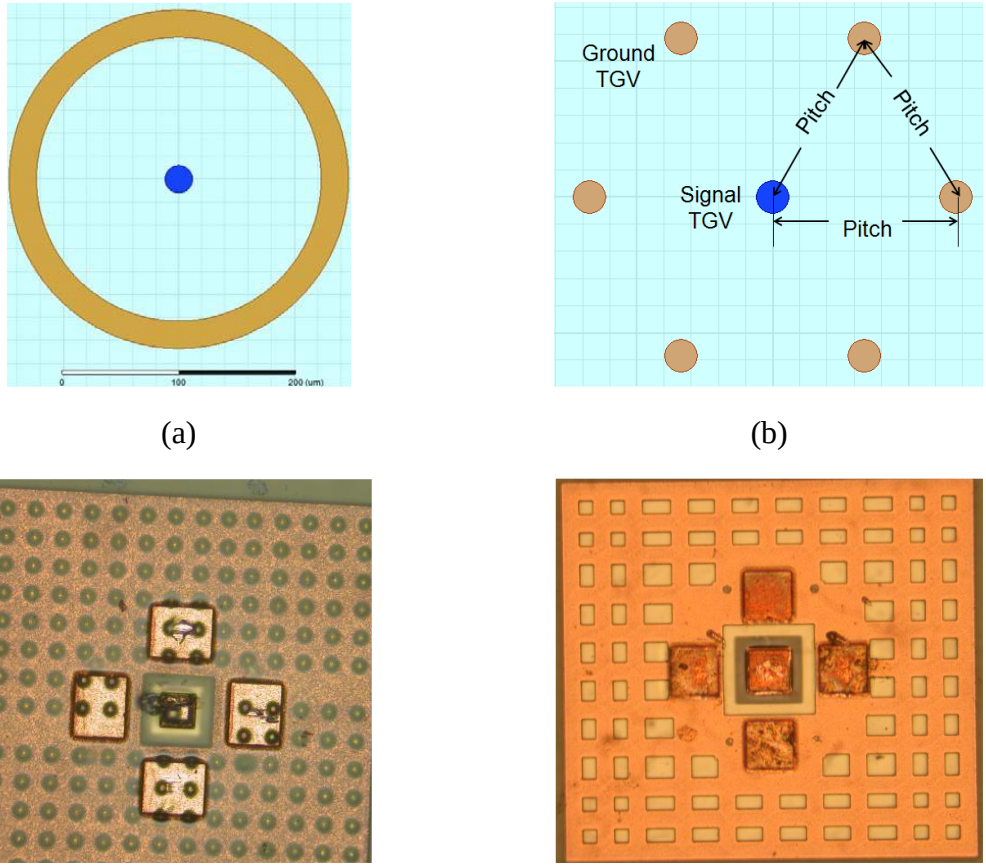


Figure 2.3: Top view of (a) coaxial TPVs in glass, (b) one signal TPV and six grounded TPVs, (c) TPVs with ground planes or signal pads, and (d) TPVs with meshed ground.

Hwang [49] from KAIST of South Korea studied the TPV-to-TPV noise coupling to a 2.4 GHz low-noise amplifier (LNA) in Radio-frequency (RF) glass interposers, as shown in Figure 2.4 (a). A modified noise figure equation was proposed to include the TPV-to-TPV noise. From the time and frequency domain simulations, it was confirmed that the LNA output waveform was distorted by the coupling noise, and with a 10 mV TPV-to-TPV noise coupling to LAN, the noise figure was degraded by 13 dB at 2 GHz, as shown in Figure 2.4 (b). In addition, Hwang [50] studied the TPV noise coupling for 2.5-D and 3D glass interposers. Equivalent circuits were proposed and validated by 3D

EM simulations in frequency domain. Finally, two methods were proposed to reduce TPV coupling noise: 1) increasing signal-to-signal TPV pitch, as shown in Figure 2.4 (c), and 2) inserting ground TPVs around signal TPVs, as shown in Figure 2.4 (d).

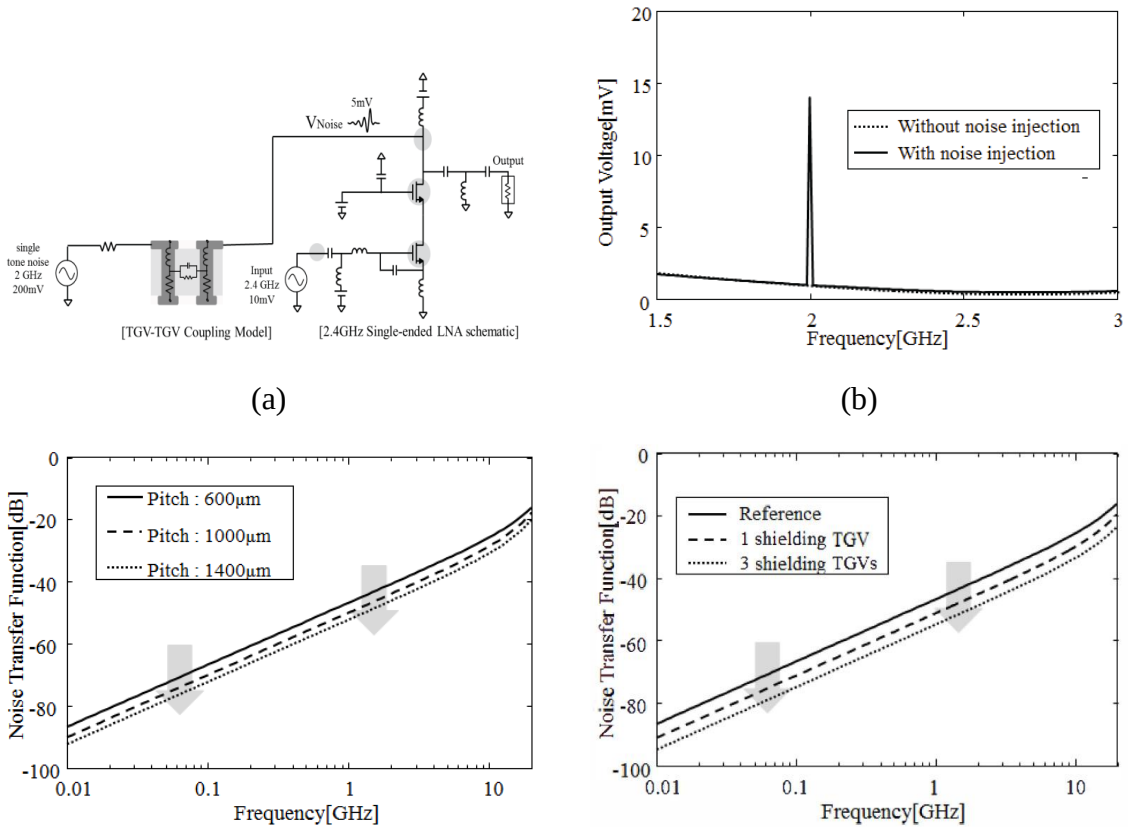


Figure 2.4: (a) Schematic view of noise coupling through TPVs to LNA, (b) simulated LNA output waveform with and without TPV coupling noise, (c) functions of noise coupling with different signal via pitch, and (d) functions of noise coupling with different numbers of inserted ground vias.

The prior art on TPV design in glass focuses on coupling noise between cylindrical TPVs. Hence, it is necessary to investigate the design guideline for tapered TPVs to minimize the impedance discontinuity and to mitigate the crosstalk for high-speed signaling.

2.3 Prior Art on Via Characterization

This section provides a brief overview of selected publications on experimental characterization of TSVs in silicon and TPVs in glass.

2.3.1 TSVs in Silicon

Prof. Joungho Kim's research group designed and characterized a high-speed single-ended TSV channel in the frequency and time domains [7, 51]. From the frequency-domain measurement, it was found that the high silicon conductance increased the loss of the TSV channel in the mid-to-high-frequency range, while the high oxide-capacitance had a negative impact on the channel loss in the low-to-mid frequency range. According to the time-domain measurement, they concluded that the interposer RDL length was the dominant factor in electrical performance, which determines the capability of a 10 Gbps data rate on TSV channel.

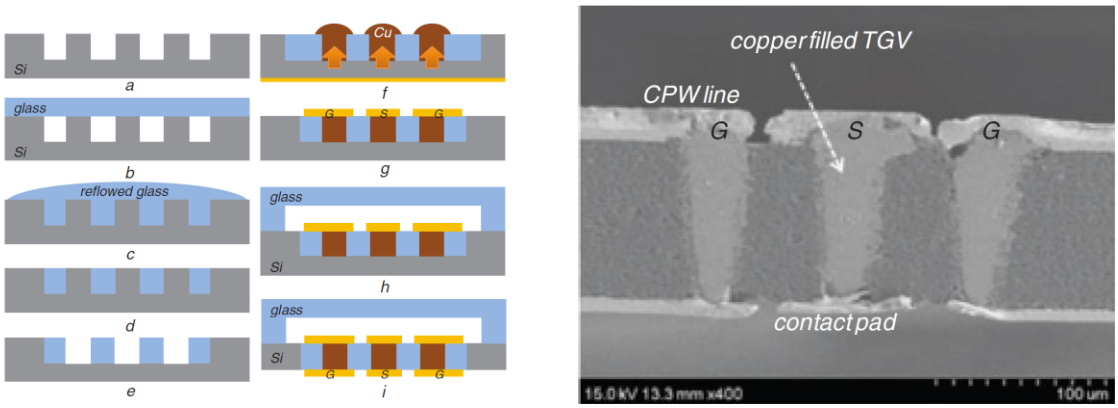
Lamy [52] from Technische Universiteit in Netherlands electrically characterized TSVs from DC to microwave frequencies. DC via resistance measurements show a good agreement with the theoretical prediction of about 16 mΩ. RF measurements up to 50 GHz showed that the inductance (53 pH) and capacitance (2.4 pF) of the TSVs were much lower than those in the case of conventional wire bonding. On the other hand, Sunohara [53] from Shinko Electric Industries and Chen [54] from Georgia Institute of Technology evaluated the electrical performance of TSVs through the measurement of *S*-parameters.

Wu [55] from Massachusetts Institute of Technology developed novel high-aspect ratio TSVs completely filled with electroplated copper. The impedance of individual vias was measured in the microwave regime using a one-port test structure, and the measured inductance was close to the theoretically expected value. Similar research was reported by Leung [56] from Hong Kong University of Science and Technology. It was found that for a single 70-μm via, the inductance and resistance were measured to be 254 pH and 0.1

Ω, respectively. In addition, the effect of via arrangements was investigated, showing that low-parasitic shorting can be obtained using multiple vias for signal transitions.

2.3.2 TPVs in Glass

Lee [57] from Dankook University of South Korea developed a novel fabrication method of copper-filled TPVs in glass for wafer-level RF MEMS packaging, as shown in Figure 2.5 (a). By using glass reflow and seedless electroplating process, a void-free copper via with a smooth side wall was achieved. Furthermore, such TPVs in Figure 2.5 (b) were applied to the packaging of a coplanar waveguide (CPW) transmission line to investigate their RF performance. The measured insertion loss of the whole package was 0.197 dB and the return loss was 20.032 dB at 20 GHz as plotted in Figure 2.6, showing little impact from TPVs.



(a) (b)

Figure 2.5: (a) Fabrication process of wafer-level RF MEMS glass packaging, and (b) SEM of copper-filled TPVs in glass.

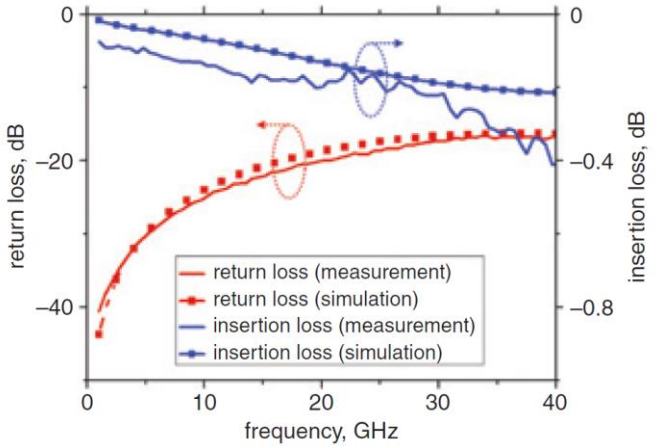
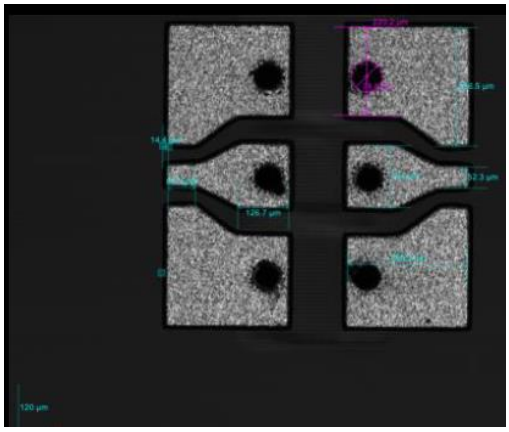
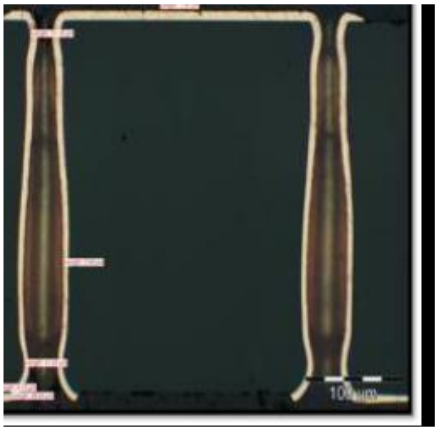


Figure 2.6: Measured and simulated RF responses of glass TPV chains.

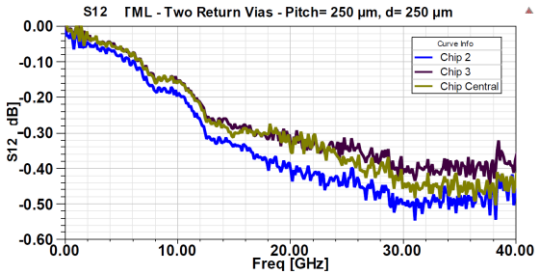
Töpper [58] from Fraunhofer IZM in Berlin characterized TPVs formed by electrical-discharge method in glass up to 40 GHz. Compared to Lee's work, this fabrication process was completely different: Töpper's process was based on widely-used processes in wafer-level packaging (WLP), namely sputtering titanium tungsten (TiW) / copper (Cu) and electroplating Cu. The top view and cross-section view of the fabricated TPVs are shown in Figure 2.7 (a) and (b), respectively. It was found from the measurement results that the CPW dual-via chain had an insertion loss and return loss of 0.35 dB and 13 dB at 20 GHz, respectively, as shown in Figure 2.7 (c) and (d).



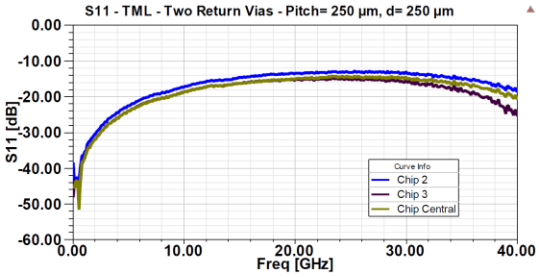
(a)



(b)



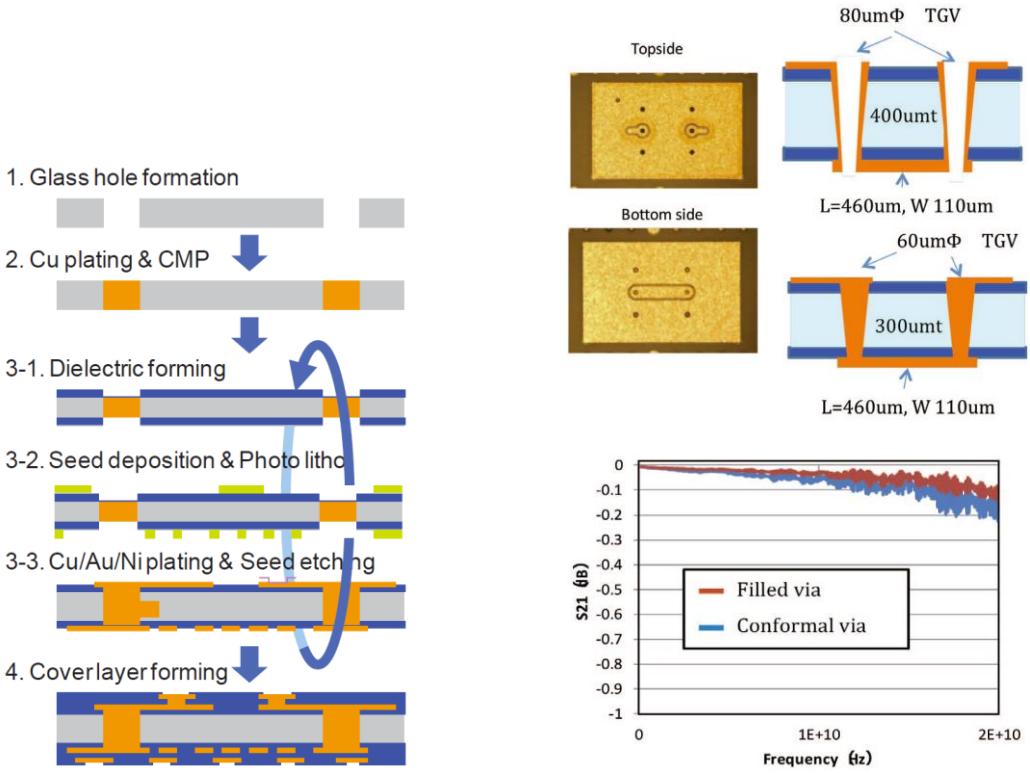
(c)



(d)

Figure 2.7: (a) Top view of fabricated dual-via chain, (b) cross-section view of TPVs filled by a conformal copper plating, (c) measurement of S_{12} till 40 GHz, and (d) measurement of S_{11} till 40 GHz.

Kuramochi [59] from Dai Nippon Printing applied a fabrication process to metallize copper-filled and conformally-plated TPVs in glass, as shown in Figure 2.8 (a). Then, the high-frequency characteristics of both types of TPVs were measured up to 20 GHz. Results shows that both types of TPVs have excellent transmission properties, and copper-filled TPVs are slightly better than conformally-plated TPVs, and the insertion loss of the CPW dual-via chain is less than 0.25 dB at 20 GHz, as shown in Figure 2.8 (b).



(a) (b)

Figure 2.8: (a) Process flow of TPV metallization in glass interposer, and (b) fabricated fully-plated and conformally-plated TPVs and the high-frequency characterization.

Two different types of processes have been demonstrated to metallize TPVs in glass, and the insertion loss of CPW dual-via chains were measured to prove the superior performance of TPVs in glass. If the TPV parasitics can be accurately characterized from the measured results, the design based on these characterized parasitic values can have a closer match to the target performance, and the design iterations can be greatly reduced.

In conclusion, even though there is an increasing amount of research on TPVs in glass, there is a critical need to develop comprehensive electrical models and design guidelines, especially at high frequencies, before glass interposers can be fully commercialized.

CHAPTER 3

ELECTRICAL MODELING OF TAPERED TPVS

This chapter presents the electrical modeling of tapered through-package vias (TPVs) in glass, addressing the fundamental challenges of modeling tapered TPVs as discussed in CHAPTER 1. A wideband scalable circuit model is proposed for tapered TPVs in glass interposers. By slicing TPVs horizontally into infinitesimally-thin pieces and integrating them along TPVs, an analytical solution was derived for the parasitic resistance (*R*) while semi-analytical expressions were derived for the parasitic inductance (*L*), capacitance (*C*) and conductance (*G*) in the proposed model. A convergence study was carried out to determine the minimum number of slices needed to discretize tapered TPVs and to achieve the desired accuracy. The proposed model was then verified against a 3D electromagnetic (EM) solver and high-frequency measurement in terms of the *S*-parameters up to 20 GHz, showing the validity of the proposed model. The sensitivity of *S*-parameters to *RLCG* values was studied, and it was found that the parasitic inductance is the most dominant factor for tapered TPVs.

In addition, the effect of the via taper on the *RLCG* parameters was comprehensively studied, and the effect of TPV metallization and fabrication processes including via sidewall roughness and polymer liners, was analyzed in terms of the electrical parameters. The via sidewall was qualitatively characterized using a scanning electron microscope (SEM) for TPVs formed by ArF excimer laser ablation [28], focused electrical-discharge method [25], and the Corning drilling method [13], and the Hammerstad model [60] was used to account for the surface roughness in the conductor loss. The polymer liner was studied by the conformal mapping method in terms of the parasitic capacitance.

Finally, a computer-aided approach was proposed to study the impact of nonlinearly tapered shapes on electrical parameters of TPVs. The parasitic resistance, loop inductance, capacitance, and conductance were computed and compared by this approach for nonlinearly tapered TPVs formed by the TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method.

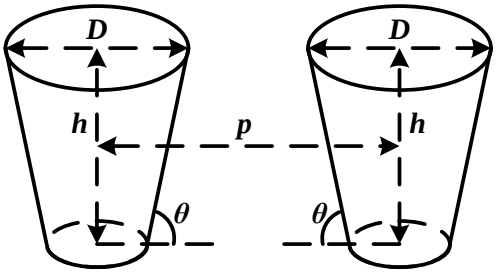
3.1 Circuit Model

TPVs in glass have a tapered shape as a result of high speed laser ablation and other commonly used via formation methods. In this section, a wideband scalable electrical model is proposed for such tapered TPVs. The closed-form equations were developed for parasitic DC and AC resistances, which compensates for the inaccuracy in [39, 43], while semi-analytical equations were presented to evaluate the parasitic inductance, capacitance and conductance. Since the circuit model is fundamentally based on electric and magnetic fields, it has validity across a wide bandwidth, as shown in Section 3.2.

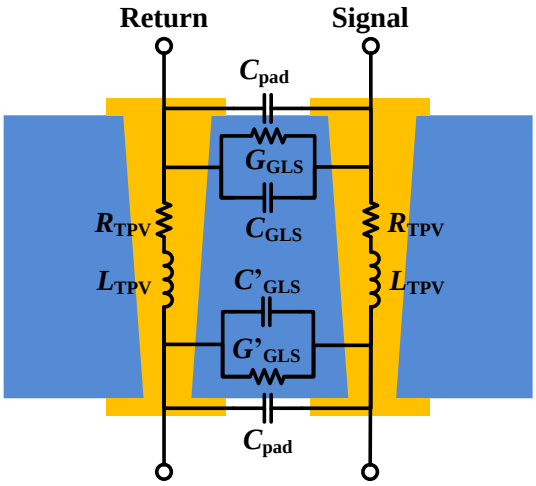
3.1.1 Modeling of Tapered TPVs

As shown in Figure 3.1 (a), a signal or return TPV has diameter d, length h, and taper angle θ, with pitch p to the adjacent TPV. Based on this geometry, Figure 3.1 (b) shows a proposed wideband scalable circuit model. Essentially, the proposed model is a lumped circuit model with parasitic resistance (R), inductance (L), capacitance (C) and conductance (G). The parasitic resistance R_{TPV} comes from the finite conductivity of the metal (typically copper) filling the vias, which increases with the square root of the frequency because of the skin effect. Due to the physical length of TPVs, there are magnetic-field lines circulating the vias when currents flow through them, introducing a parasitic loop inductance L_{TPV} residing in the signal and return vias. Apart from the magnetic-field lines, the electric-field lines start from the signal TPV and terminate at the

return TPV, resulting in a total substrate capacitance which is the sum of C_{GLS} and C'_{GLS} in the model. In addition to the parasitic capacitance, a parasitic conductance, as the sum of G_{GLS} and G'_{GLS}, is induced and it is attributed to the polarization of the molecules in glass under the applied electric field. Compared to the π-shape circuit presented in [42], the proposed model is not affected by the parasitics of traces. Detailed computation of each component in the model is presented in Subsection 3.1.2.



(a)



(b)

Figure 3.1: (a) Perspective view of tapered TPV geometry, and (b) proposed wideband scalable circuit model for a TPV pair consisting of a signal TPV and a return TPV.

It is well-known that as long as the physical size of any object is less than one tenth of the wavelength, the object can be considered as electrically small and it then can

be accurately modeled as lumped circuits. As for TPVs, the length of the vias is in the micrometer region corresponding to the wavelength of a few hundred GHz in glass. Consequently, the proposed circuit model will be sufficiently accurate over a very wide bandwidth up to a few tens of GHz, because the TPV length is still electrically short compared to the wavelength in the glass. Furthermore, the computation of the parasitic *RLCG* model, which will be discussed later on in this chapter, uses the geometric parameters of TPVs, implying that the model is scalable to different TPV dimensions.

3.1.2 Computation of Parasitic *RLCG*

Parallel wires, also known as a two wire transmission line, with a uniform cross section along the wires, have exact closed-form equations for the transmission-line parameters [61, 62]. If tapered TPVs are sliced horizontally into many pieces as shown in Figure 3.2, utilizing these equations can provide an approximate evaluation of the parasitic *RLCG* parameters in the proposed model. When these pieces become infinitesimally thin, indicating an infinite amount of slices, the parasitic *RLCG* values computed by this method will approach those of the tapered TPVs.

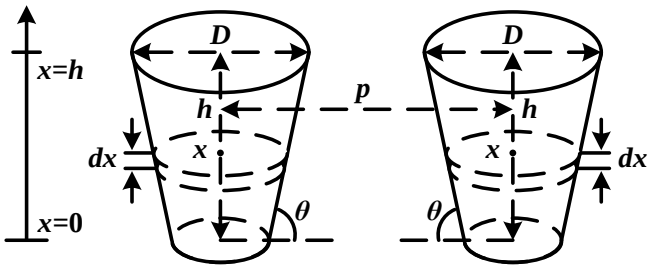


Figure 3.2: Schematic diagram of tapered TPVs, illustrating the scheme of computing the parasitic *RLCG* values.

Using this approach, the parasitic DC resistance value of a TPV fully filled with copper can be calculated from

$$
\begin{aligned}
R_{\text{TPV, DC}} &= \int_0^h \rho \cdot \frac{dx}{\pi \cdot r_x^2} \\
&= \int_0^h \rho \cdot \frac{dx}{\pi \cdot \left(D/2 - (h-x)/\tan\theta\right)^2} \\
&= \frac{4\rho}{\pi} \cdot \frac{h}{D \cdot \left(D - 2h/\tan\theta\right)}
\end{aligned} \tag{3.1}
$$

where ρ is the resistivity of the copper filling the via, and r_x is the radius of the via at the vertical position x as shown in Figure 3.2. As the taper angle θ ramps up to 90°, the DC resistance value becomes

$$
R_{\text{TPV, DC}}\Big|_{90^\circ} = \frac{4\rho}{\pi} \cdot \frac{h}{D^2} \tag{3.2}
$$

which is consistent with the cylindrical via equation provided in [39]. Further verification of this equation will be presented in Section 3.2.

The parasitic AC resistance value can be calculated in a similar way, but due to the skin effect, the current tends to flow on the surface, which should be taken into consideration. It is important to mention that if the skin depth is larger than the via diameter, all the copper is still used to conduct current, which was ignored by the authors in [39, 43]. So, the parasitic AC resistance value is expressed as

$$
R_{\text{TPV, AC}} = \begin{cases}
\dfrac{\rho \cdot x_0}{\pi} \cdot \left(\dfrac{D}{2} - \dfrac{h}{\tan\theta}\right)^{-1} \cdot \left(\dfrac{D}{2} - \dfrac{h - x_0}{\tan\theta}\right)^{-1} \\
\qquad + \dfrac{\rho}{2\pi\delta_s} \cdot \tan\theta \cdot \ln\left(1 - \dfrac{2}{\tan\theta} \cdot \dfrac{h - x_0}{D - \delta_s}\right)^{-1}, & \text{if } x_0 > 0 \\
\dfrac{\rho}{2\pi\delta_s} \cdot \tan\theta \cdot \ln\left(1 - \dfrac{2}{\tan\theta} \cdot \dfrac{h}{D - \delta_s}\right)^{-1}, & \text{if } x_0 < 0
\end{cases} \tag{3.3}
$$

where x_0 is the vertical position at which the radius is equal to the skin depth δ_s, and it is calculated as

$$
x_0 = h - \tan\theta \cdot \left(D/2 - \delta_s\right). \tag{3.4}
$$

If x_0 is positive, it implies that there is indeed a vertical point below which the radius of the via is smaller than the skin depth δ_s and all the copper is utilized to conduct current. Otherwise, if x_0 is negative, the AC current is concentrated in the annular surface. In the case of a straight TPV with a large radius, the AC resistance value is then

$$R_{\text{TPV, AC}}\big|_{90^o} = \frac{\rho}{\pi} \cdot \frac{h}{\delta_s \cdot (D - \delta_s)} \tag{3.5}$$

which is consistent with the formula in [39].

Then, the values for the parasitic loop inductance and the parasitic capacitance can be calculated as

$$\begin{aligned} L_{\text{TPV}} &= \frac{\mu_0 \mu_r}{\pi} \cdot \int_0^h \cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2(h-x)} \right) dx \\ &\approx \frac{\mu_0 \mu_r}{\pi} \cdot \sum_{i=1}^{N} \cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2h(N-i)/N} \right) \cdot \frac{h}{N} \end{aligned} \tag{3.6}$$

$$\begin{aligned} C_{\text{GLS}} &= \pi\varepsilon_0\varepsilon_r \cdot \int_{h/2}^{h} \left[\cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2(h-x)} \right) \right]^{-1} dx \\ &\approx \pi\varepsilon_0\varepsilon_r \cdot \sum_{i=1}^{N} \left[\cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2h(N-i)/(2N)} \right) \right]^{-1} \cdot \frac{h}{2N} \end{aligned} \tag{3.7}$$

$$\begin{aligned} C'_{\text{GLS}} &= \pi\varepsilon_0\varepsilon_r \cdot \int_0^{h/2} \left[\cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2(h-x)} \right) \right]^{-1} dx \\ &\approx \pi\varepsilon_0\varepsilon_r \cdot \sum_{i=1}^{N} \left[\cosh^{-1}\left(\frac{p \cdot \tan\theta}{D \cdot \tan\theta - 2h(2N-i)/(2N)} \right) \right]^{-1} \cdot \frac{h}{2N} \end{aligned} \tag{3.8}$$

where N is the number of the slices, μ_0 and ε_0 are the vacuum permeability and permittivity, respectively, and μ_r and ε_r are the relative permeability and permittivity of the glass. The integrals in (3.6)-(3.8) are based on the transmission line parameters for two wires [62]. The integral in (3.6) is used to calculate the loop inductance of the tapered TPV pair, while the integrals in (3.7) and (3.8) are used to calculate the top half and the bottom half of the tapered TPV pair. Closed-form equations cannot be obtained for the integral, yet the discretized ones will give a reasonably accurate approximation.

The convergence in (3.6), (3.7), and (3.8) with various N values will be discussed in Subsection 3.1.3, and the results show that when N is larger than 10, the convergence error is below 10%; and when N is 20, it is about 2%. Thus, N was chosen to be 50 herein to achieve a convergence error of less than 0.5%.

Afterward, the conductance value is calculated using the following relation with the capacitance

$$G_{\mathrm{GLS}} = \omega C_{\mathrm{GLS}} \cdot \frac{\varepsilon''}{\varepsilon_r} \tag{3.9}$$

$$G'_{\mathrm{GLS}} = \omega C'_{\mathrm{GLS}} \cdot \frac{\varepsilon''}{\varepsilon_r} \tag{3.10}$$

where ε'' is equal to $\varepsilon_r \times \tan\delta$, and tan δ is the loss tangent of the glass.

Finally, the capacitance value of the via pads is calculated by the two-wire transmission line model [62]

$$C_{\mathrm{pad}} = \frac{\pi \varepsilon_0 \varepsilon_{r,\mathrm{k}} t_{cu}}{\cosh^{-1}\left(p / D_{pad}\right)} \tag{3.11}$$

where $\varepsilon_{\mathrm{r,\,k}}$ is the relative permittivity of the dielectric layer on the top and at the bottom of the vias, t_{cu} is the copper thickness of the pads, and D_{pad} is the diameter of the pads capturing the TPVs.

Thus far, each component in the proposed circuit model can be calculated either by analytical equations or by semi-analytical ones. The proposed circuit model will be verified in the next section by both simulation and measurement.

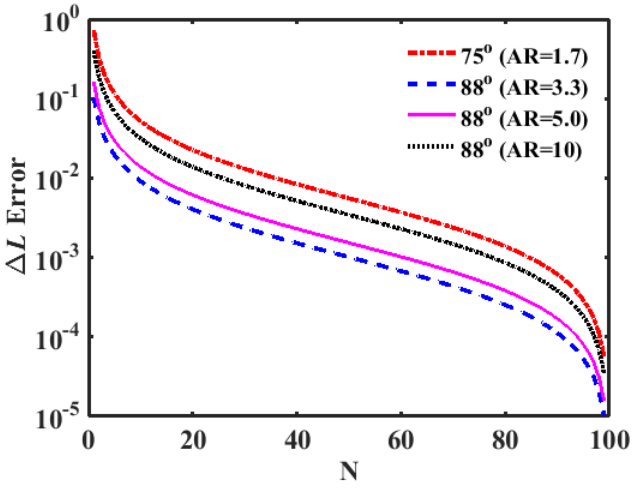
3.1.3 Convergence Study

The relative convergence error is defined as

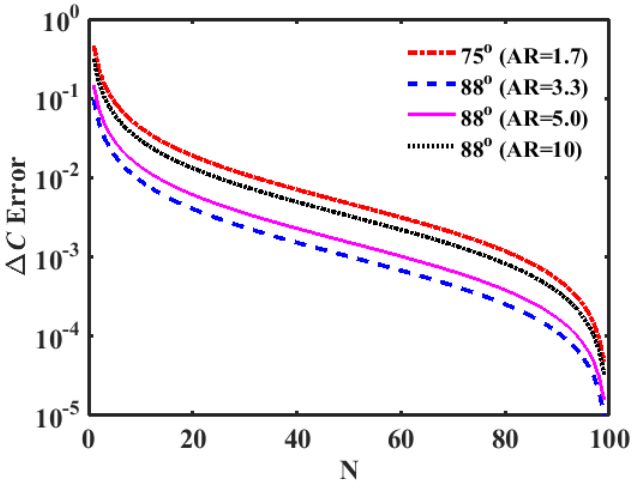
$$\frac{\Delta L}{L_{\max}} = \frac{\left|L_N - L_{\max}\right|}{L_{\max}} \tag{3.12}$$

$$\frac{\Delta C}{C_{\max}} = \frac{\left|C_N - C_{\max}\right|}{C_{\max}} \tag{3.13}$$

where L_N and C_N are the computed loop inductance and capacitance for the N^{th} slice respectively, while L_{max} and C_{max} are the computed loop inductance and capacitance for a large number of slices, respectively. The relative convergence errors of the loop inductance and capacitance are plotted as a function of the slice number N in Figure 3.3 (a) and (b), respectively, for the case of 30-μm-diameter TPVs with various aspect ratios (ARs) and taper angles.



(a)



(b)

Figure 3.3: Relative convergence error as a function of the slice number for (a) the parasitic inductance, and (b) capacitance.

In Figure 3.3, the slice number N is varied from 1 to 100. Since the conductance G was computed based on the capacitance C by (3.9) and (3.10), the convergence of the conductance G is identical to that of the capacitance C. It can be seen from Figure 3.3 that, as stated before, when N is larger than 10, the relative convergence error is below 10%; and when N is 20, it is about 2%. Herein, N was chosen to be 50, resulting in about 0.5% relative convergence error. In addition, it is found that as the taper angle decreases and the aspect ratio increases, the relative convergence error increases, indicating that more tapered TPVs have lower convergence rate.

3.2 Model Verification

To verify the validity and the scalability of the proposed TPV circuit model, the *S*-parameters computed by this circuit model were compared against the *S*-parameters from the 3D EM solver (HFSS) and the measured *S*-parameters from the fabricated test vehicle. As the International Technology Roadmap for Semiconductors (ITRS) projected the scaling trend for the coarse TSVs for the die-to-ball interconnection [1], which is presented in Table 3.1, this roadmap was used in this section to verify the proposed circuit model for parametric TPV variations. The glass substrate used in this section has a dielectric constant of 5.3 and a loss tangent of 0.006 at 10 GHz, while the annealed copper has a conductivity of 5.8×10^7 S·m. It will be shown that the proposed model computes the *S*-parameters of TPVs as accurately as the 3D EM solver but with much less computational time, and they agree very well with the measured results.

Table 3.1: Coarse TPV roadmap

Year	2011	2013	2015	2017	2019	2021	2023
p (μm)	100	90	80	60	60	40	36
D (μm)	60	50	40	30	30	20	18
AR	1.4	1.5	1.6	1.6	1.6	1.6	1.6

3.2.1 *S*-Parameters Computation

The proposed model is essentially a π-shape circuit that can be easily analyzed by *ABCD*-parameters, and the *ABCD*-parameters are then converted to *S*-parameters for the next comparison. Using the equations provided in [62], the *ABCD*-parameters can be calculated as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+Y_2/Y_3 & 1/Y_3 \\ Y_1+Y_2+Y_1\cdot Y_2/Y_3 & 1+Y_1/Y_3 \end{bmatrix} \tag{3.14}$$

with

$$Y_1 = j\omega\left(C_{\text{pad}} + C_{\text{GLS}}\right) + G_{\text{GLS}} \tag{3.15}$$

$$Y_2 = j\omega\left(C_{\text{pad}} + C'_{\text{GLS}}\right) + G'_{\text{GLS}} \tag{3.16}$$

$$Y_3 = \left(2\cdot k_p \cdot R_{\text{TPV}} + 2\cdot k_p \cdot j\omega L_{\text{TPV}}\right)^{-1} \tag{3.17}$$

where ω is the angular frequency, k_p is proximity factor which can be found in [63], and the other terms can be calculated using the aforementioned equations. The termination for the *S*-parameters computation is set to the commonly-used 50 Ω.

3.2.2 Model-to-Simulation Correlation

Basically, four geometric parameters determine the electrical parasitics of the tapered TPVs: diameter, length, pitch, and taper angle. Three scenarios were carefully compared between the proposed model and the 3D EM solver.

In the first scenario, the following TPVs were computed by the proposed model and also simulated in the 3D EM solver: straight TPVs of 18/30/60 μm diameters at minimum pitches, where the aspect ratios of 30-μm TPVs were varied as 1.7, 3.3, and 5.0, while the aspect ratios of 18-/60-μm TPVs were kept as 1.7. By doing so, the scalability of the proposed model in terms of TPV diameter and length could be verified. The magnitude and the phase of S_{21} from the proposed model and the 3D EM solver are depicted in Figure 3.4 (a) and (b), respectively.

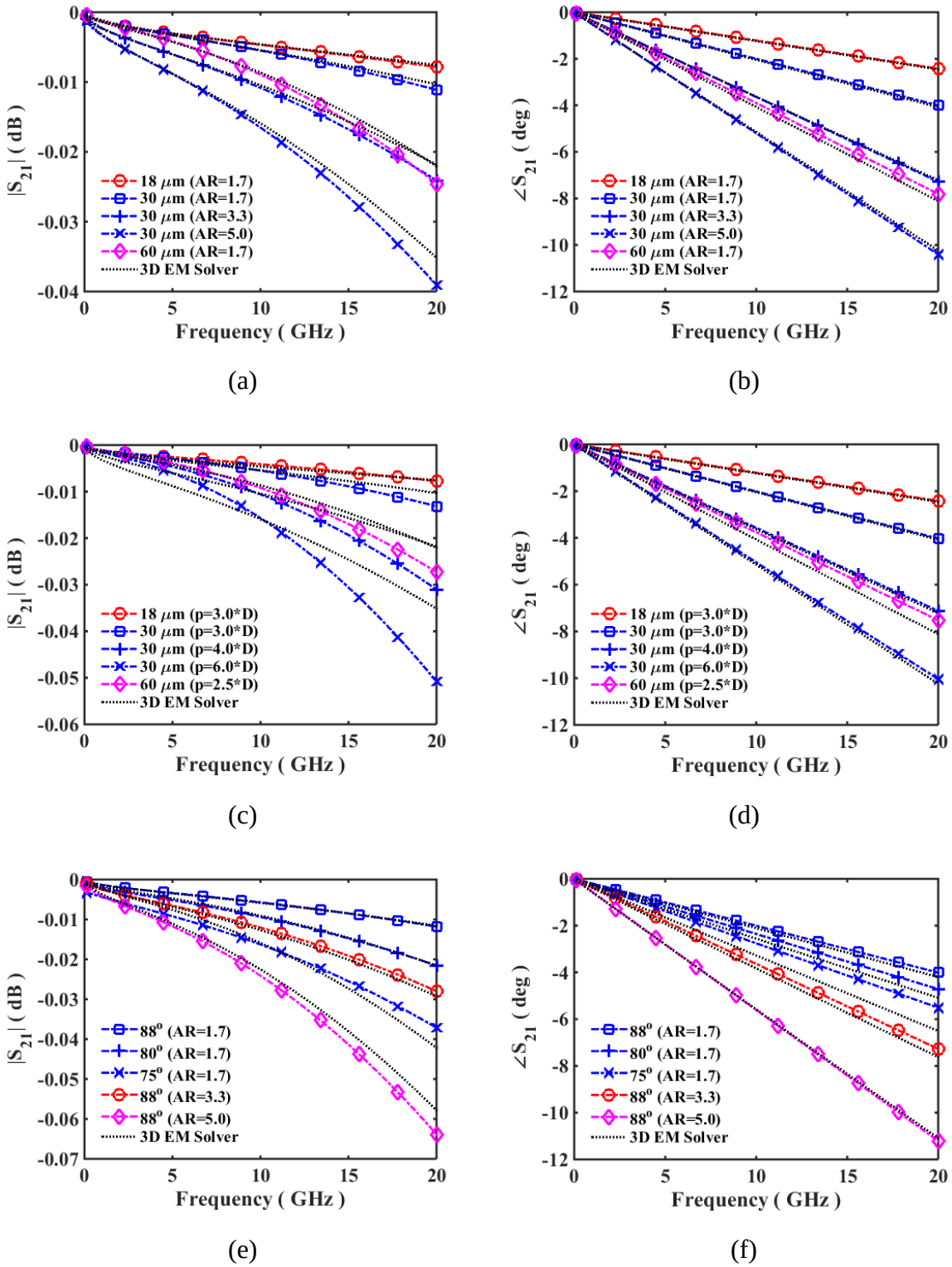


Figure 3.4: *S*-parameter comparison of TPVs with different dimensions in glass between the proposed model and the 3D EM Solver: (a) S_{21} magnitude, (b) S_{21} phase

of 18-/30-/60-µm-diameter straight TPVs with 1.7/3.3/5.0 aspect ratios (ARs) at minimum pitches; (c) S_{21} magnitude, and (d) S_{21} phase of 18-/30-/60-µm-diameter straight TPVs with 1.7 aspect ratio at various pitches; (e) S_{21} magnitude, and (f) S_{21} phase of 30-µm-diameter tapered TPVs with 1.7/3.3/5.0 aspect ratios and 75º/80º/88º taper angles at minimum pitch.

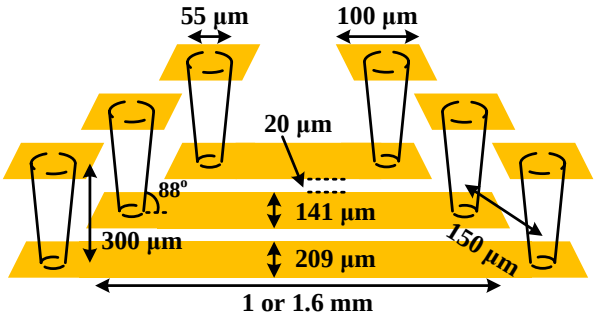
The second scenario considered TPVs of different diameters and different pitches. Specifically, straight TPVs of 18/30/60 µm diameters were kept to be of 1.7 aspect ratio, but the pitches were varied from 2.5×*D* up to 6×*D*. Thus, the scalability of TPV pitch in the proposed model was verified. In Figure 3.4 (c) and (d), the magnitude and the phase of S_{21} computed by the proposed model and the 3D EM solver are presented.

The last scenario was to verify the proposed model for various taper angles. Thus, 30-µm tapered TPVs of various aspect ratios and of various taper angles were compared in terms of S_{21} which was computed either by the proposed model or by the 3D EM solver as shown in Figure 3.4 (e) and (f). It can be seen in Figure 3.4 (a)~(f) that the magnitude, as well as the phase obtained from the proposed circuit model matches closely to that from the 3D EM solver. The maximum magnitude difference is about 0.01 dB while the maximum phase difference is about 1 deg, which is negligible. In addition to S_{21}, S_{11} and S_{22} were also compared between the proposed model and 3D EM solver, and they also showed excellent agreement with each other.

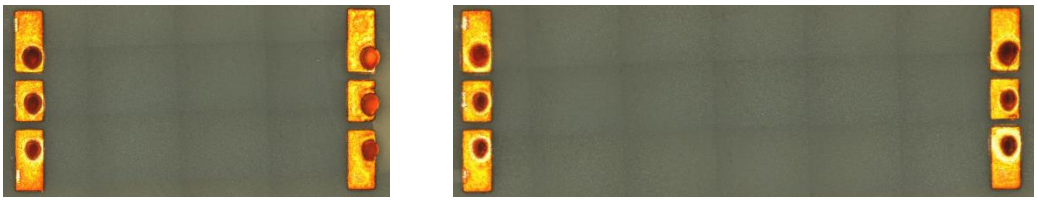
3.2.3 Model-to-Hardware Correlation

Due to the limited glass suppliers and TPV formation methods accessible to the author, the proposed model was experimentally verified for one type of tapered TPV. Dual-via chains are commonly used to experimentally evaluate the TPV performance. Two chains of different lengths were designed here in 300-µm-thick EN-A1 glass from Asahi Glass Company, Tokyo, Japan [25], with 55-µm via diameter at the entrance and

150-µm center-to-center via pitch, as shown in Figure 3.5 (a). The TPVs were formed by a focused electrical discharge micro-machining method with an 88° taper angle. The bottom CPW transmission line in these two chains were designed to match to 50 Ω impedance, with a signal conductor width of 141 µm, a ground conductor width of 209 µm, a gap between signal and ground conductors of 20 µm, and a length of either 1 mm or 1.6 mm, which is also illustrated in Figure 3.5 (a). These two via chains were metallized using a semi-additive copper plating process, and they were measured using a Vector Network Analyzer (VNA) and the Ground-Signal-Ground (GSG) probes. Figure 3.5 (b) shows the stitched top view of the fabricated 1.0 mm and 1.6 mm dual-via chains. Careful observation reveals that some TPVs were misaligned from the pad centers. In addition, the corresponding GSG TPV circuit model was constructed and the *S*-parameters were computed by the proposed model. The bottom CPW transmission lines were simulated in a 3D EM solver, and then were cascaded with the proposed TPV circuit model.



(a)

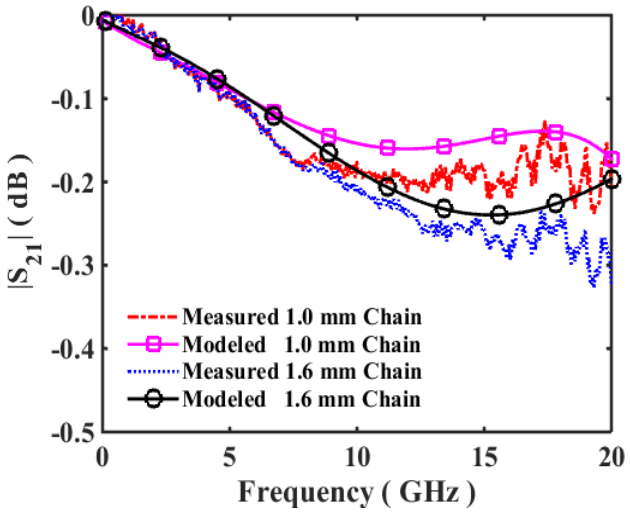


(b)

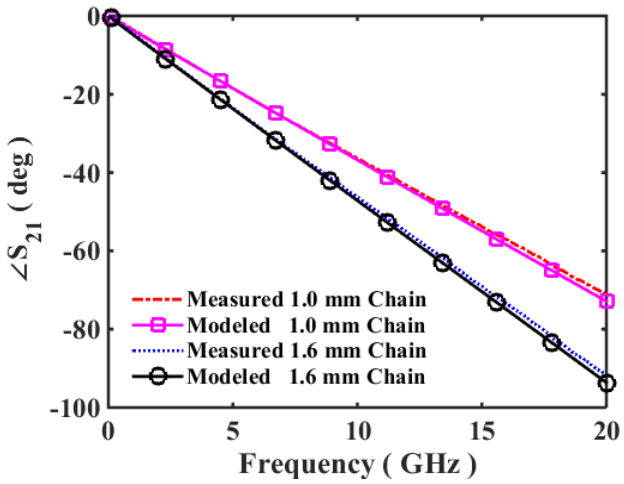
Figure 3.5: (a) The schematic diagram of the designed dual-via chain with all the structural parameters labeled, and (b) the stitched top view of the fabricated 1.0

mm and 1.6 mm dual-via chains, in which the bottom CPW transmission lines are not visible.

The measured and the modeled results are shown in Figure 3.6 in terms of the S_{21} magnitude and the S_{21} phase. It can be seen that the measured results of the 1.0 mm and 1.6 mm chains correlate closely with those from the proposed model, especially the S_{21} phase. The maximum error for S_{21} magnitude is about 0.05 dB below 20 GHz, while that for S_{21} phase is around 2 deg. These negligible errors might come from the exact probing position during the measurement, which is explained in detail in [16]. There are a few ripples in the measured S_{21} magnitude, which could be attributed to the misalignment in the fabrication and the calibration in the measurement. Thus, we can establish the validity and the scalability of the proposed model based on the above comparison.



(a)

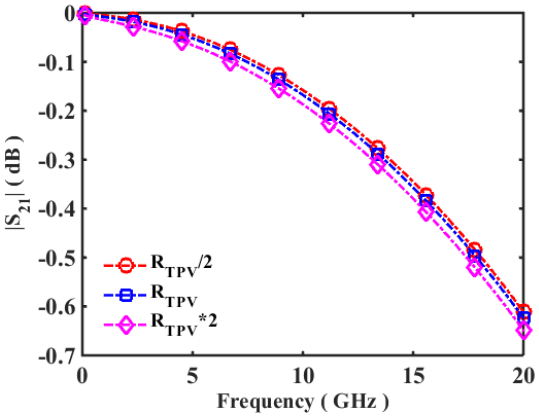


(b)

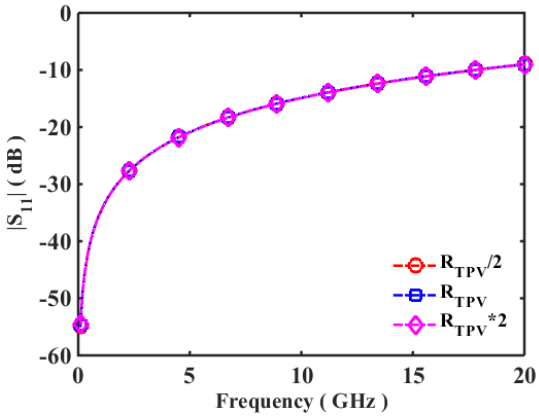
Figure 3.6: *S*-parameter comparison between the proposed model and the measurement of the fabricated two dual-via chains: (a) S_{21} magnitude, (b) S_{21} phase.

3.2.4 Sensitivity Study on *RLCG*

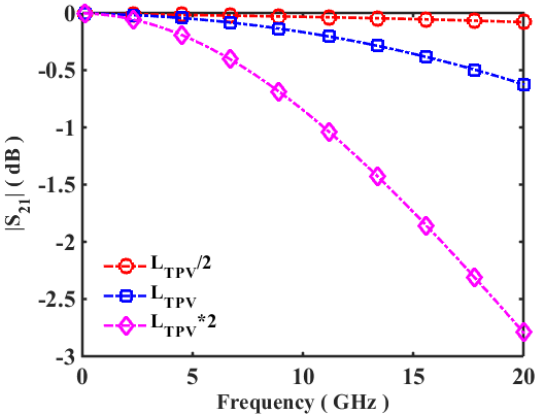
The sensitivity of *S*-parameters with respective to the parasitic resistance, inductance, conductance and capacitance was studied, and the results are plotted in Figure 3.7. The scenario of fabricated TPVs with 55-µm diameter, 366-µm length and 88° taper angle was analyzed. By comparing both the S_{21} and S_{11} magnitudes, it is observed from Figure 3.7 that the parasitic resistance and conductance do not significantly affect the *S*-parameters, while the parasitic inductance and capacitance significantly affect the *S*-parameters. From the comparison between Figure 3.7 (c) and (e), and also (a) and (g), we can see that *S*-parameters are more sensitive to the inductance than the capacitance. Therefore, the parasitic inductance, capacitance, resistance, and conductance have the first, second, third, and fourth most pronounced impacts on *S*-parameters, respectively.


|S21| (dB)
Frequency (GHz)
RTPV/2
RTPV
RTPV*2

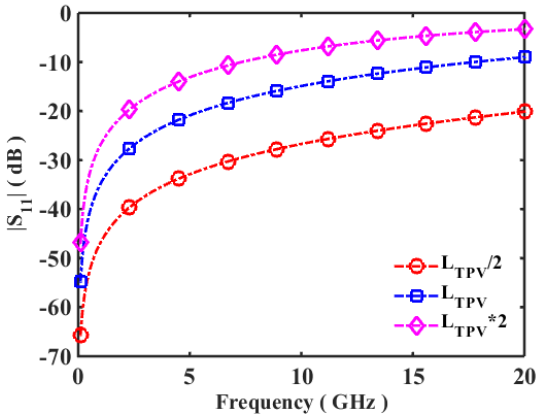
(a)


|S11| (dB)
Frequency (GHz)
RTPV/2
RTPV
RTPV*2

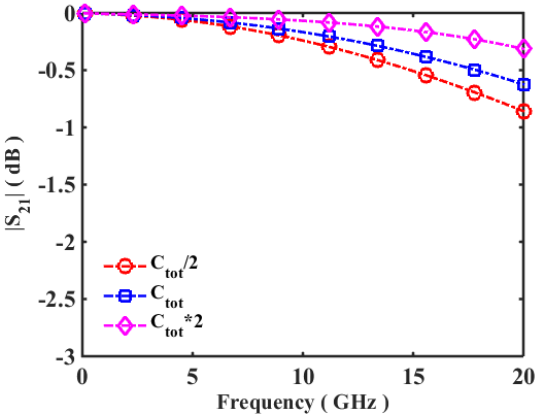
(b)


|S21| (dB)
Frequency (GHz)
LTPV/2
LTPV
LTPV*2

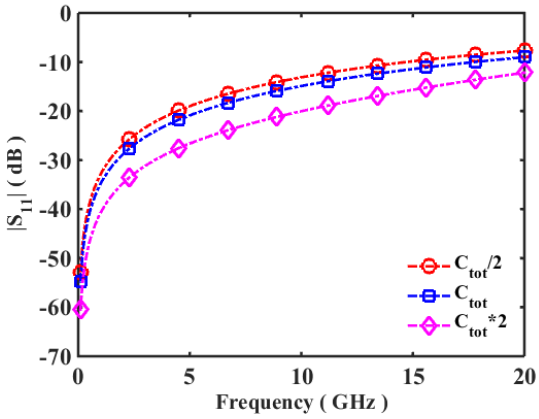
(c)


|S11| (dB)
Frequency (GHz)
LTPV/2
LTPV
LTPV*2

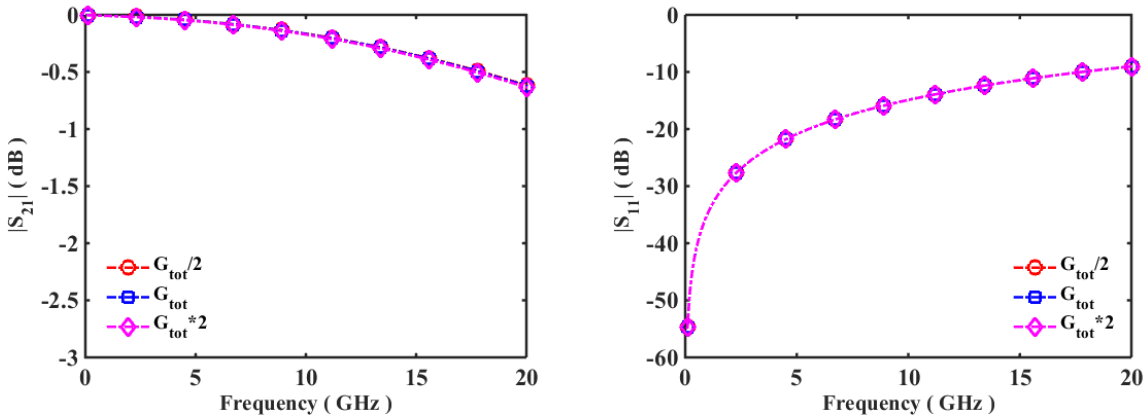
(d)


|S21| (dB)
Frequency (GHz)
Ctot/2
Ctot
Ctot*2

(e)


|S11| (dB)
Frequency (GHz)
Ctot/2
Ctot
Ctot*2

(f)



(g) (h)

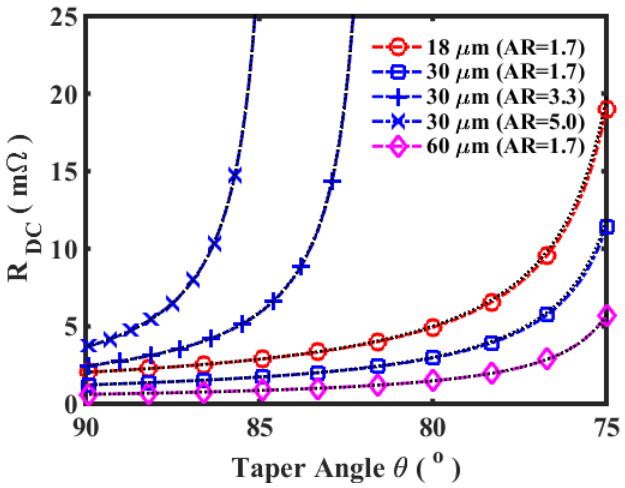
Figure 3.7: Magnitude of (a) S_{21} and (b) S_{11} for varying resistance; magnitude of (c) S_{21} and (d) S_{11} for varying inductance; magnitude of (e) S_{21} and (f) S_{11} for varying capacitance; magnitude of (g) S_{21} and (h) S_{11} for varying conductance.

3.3 Analysis of Taper Effect

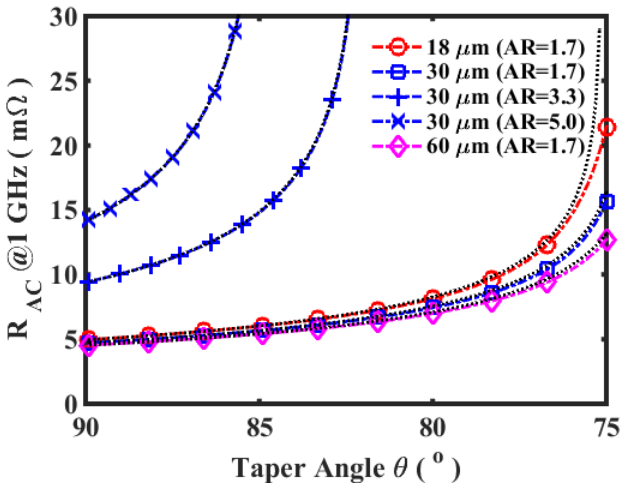
After the proposed model was verified by comparing it with the 3D EM solver and the measurements from the fabricated test vehicles, it is of interest to comprehensively study the taper effect on each component in the model, given various taper angles from different drilling methods. In this section, the adverse effect of via taper on the resistance, inductance, capacitance, and conductance will be discussed.

3.3.1 Taper Effect on Resistance and Inductance

The DC resistance value, as well as the 1 GHz resistance value of tapered TPVs calculated by (3.1) and (3.3) respectively, are depicted in Figure 3.8, where the taper angles decrease from 90^{o} to 75^{o}. The TPV diameters were varied as 18, 30 and 60 μm, while the aspect ratios were varied as 1.7, 3.3 and 5.0 in Figure 3.8. Additionally, the DC and 1 GHz resistances were calculated using the equations derived in [39] for comparison.



(a)



(b)

Figure 3.8: (a) DC resistance values and (b) 1 GHz resistance values of TPVs vary with taper angles for 18-/30-/60-µm-diameter TPVs with 1.7/3.3/5.0 aspect ratios. The dashed lines represent the results from [39].

Both the DC and 1 GHz resistance values increase with decreasing taper angles, and the increasing rate for the high aspect-ratio TPVs is higher than that for low aspect-ratio ones. To quantitatively analyze the taper effect on the resistances, the variances between the tapered TPVs and straight ones were derived using (3.1)-(3.5).

The relative DC resistance variance is expressed as

$$\frac{\Delta R_{\text{TPV, DC}}}{R_{90^o}} = \frac{R_{\text{taper}} - R_{90^o}}{R_{90^o}} = \left(\frac{\tan\theta}{2 \cdot \text{AR}} - 1 \right)^{-1}. \tag{3.18}$$

Thereby, it can be concluded that the relative DC resistance variance depends on two parameters: the taper angle θ and the aspect ratio (AR). For a fixed aspect ratio, as taper angle θ increases, the DC resistance value of tapered TPVs approaches that of straight TPVs, which is intuitively evident. If the aspect ratio of TPVs becomes higher for a given taper angle, this variance increases, which means the tapered TPVs deviate from the straight TPVs value.

In the same way, the relative AC resistance variance is

$$\frac{\Delta R_{\text{TPV, AC}}}{R_{90^o}} = \frac{\tan\theta \cdot \ln\left(1 - \frac{2}{\tan\theta} \cdot \frac{h}{D - \delta_s} \right)^{-1}}{2h/(D - \delta_s)} - 1. \tag{3.19}$$

When the skin depth δ_s is small compared with the TPV diameter D, which is usually true at high frequencies, (3.19) can be simplified as

$$\frac{\Delta R_{\text{TPV,AC}}}{R_{90^o}} \approx \frac{\tan\theta \cdot \ln\left(1 - \frac{2}{\tan\theta} \cdot \text{AR} \right)^{-1}}{2 \cdot \text{AR}} - 1. \tag{3.20}$$

If the Taylor series was applied to the natural logarithm in the above equation, (3.20) can be reshaped into an explicit form as below

$$\frac{\Delta R_{\text{TPV, AC}}}{R_{90^o}} = \frac{R_{taper} - R_{90^o}}{R_{90^o}} \approx \frac{1}{3} \cdot \frac{(2 \cdot \text{AR})^3}{\tan^2\theta} - \frac{1}{5} \cdot \frac{(2 \cdot \text{AR})^5}{\tan^4\theta} + \cdots. \tag{3.21}$$

Comparing (3.18) with (3.21) enlightens us that the relative AC resistance variance also depends on two parameters: the taper angle θ and the aspect ratio (AR), but with higher-order nonlinear relationship than the DC resistance variance. Thanks to this higher-order nonlinear relationship, the AC resistance variance is less influenced by the taper effect. Table 3.2 presents the computed relative resistance variance for 30-μm-

diameter TPVs of various taper angles and aspect ratios. In each row, the AC resistance variance is less than the DC resistance variance, as predicted above; in each column, the resistance variance increase with increasing aspect ratio for a given taper angles.

Table 3.2: Relative resistance variance of 30-μm diameter TPVs

TPV	DC	1 GHz	10 GHz
75^{o} (AR=1.7)	835.47%	233.22%	167.65%
80^{o} (AR=1.7)	142.43%	58.08%	52.83%
88^{o} (AR=1.7)	13.11%	6.80%	6.44%
88^{o} (AR=3.3)	30.19%	15.02%	14.14%
88^{o} (AR=5.0)	53.39%	25.25%	23.60%

Another adverse effect of the via taper is on the loop inductance. Since only a discretized expression was provided in this chapter, a few scenarios were calculated for different TPV dimensions and the results are presented in Figure 3.9. It can be seen that the inductance of the tapered TPVs increases with decreasing taper angles θ for a constant aspect ratio and TPV diameter, and it increases with increasing aspect ratio for a constant taper angle and TPV diameter. Detailed data analysis on the inductance shows that the maximum increase of the inductance is around 80%.

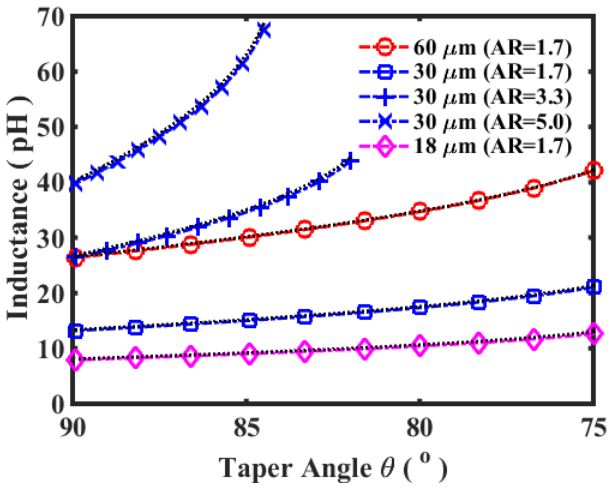


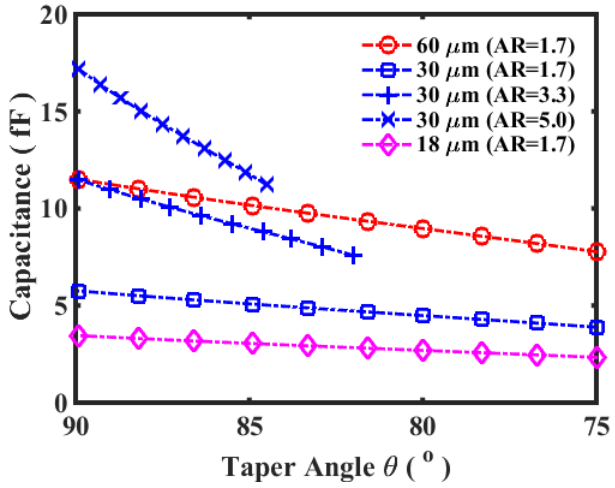
Figure 3.9: Loop inductance values of TPVs vary with taper angles for 18-/30-/60-µm-diameter TPVs with 1.7/3.3/5.0 aspect ratios. The dashed lines represent the results from [39].

Fundamentally, there are two reasons for such a taper effect on the TPV inductance. Since the inductance in the proposed model is the loop inductance the actual signal sees, it consists of two parts, namely the self-inductance and the mutual inductance. As the current travels from the top down to the bottom of the TPV, the diameter decreases along the TPV because of the taper, causing the self-inductance to increase. In addition to this, the adjacent return TPV is further separated away from the signal TPV, when the signal travels down along the tapered TPVs. Thus, the mutual inductance between the signal TPV and the return TPV, which is beneficial to reduce the loop inductance, decreases for the tapered TPVs.

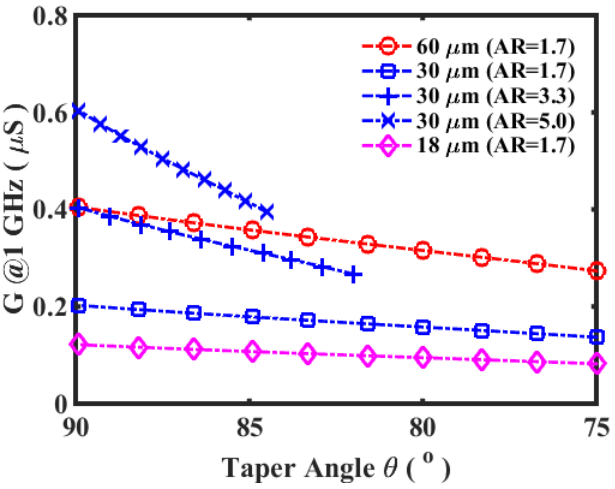
From this investigation of via taper on the resistance and inductance, two conclusions can be made: 1) Both the DC and AC resistances increase with decreasing taper angles, and the DC resistance is more impacted by the via taper than the AC resistance. 2) The inductance also increases with decreasing taper angles, while the maximum increase is about 80%.

3.3.2 Taper Effect on Capacitance and Conductance

The total capacitance and conductance can be expressed as $C = C_{GLS} + C'_{GLS}$ and $G = G_{GLS} + G'_{GLS}$, respectively. Since no closed-form expressions exist for the capacitance and the conductance, the scenarios in Subsection 3.3.1 were computed, with the results given in Figure 3.10.



(a)



(b)

Figure 3.10: (a) Capacitance values and (b) 1 GHz conductance values of TPVs vary with taper angles for 60-/30-/18-μm-diameter TPVs with 1.7/3.3/5.0 aspect ratios.

As observed in Figure 3.10, both the capacitance and the conductance decrease with decreasing taper angles. Quantitative analysis shows that this capacitance and conductance reduction is about 40% for a taper angle of 75^{o}. Another observation is that as the aspect ratio increases for a certain taper angle and TPV diameter, the rate of decrease of the capacitance and the conductance becomes faster. In other words, the tapered TPVs have smaller capacitance and conductance than the straight ones. The reason is that the taper separates the bottom of the TPVs from the adjacent TPVs, resulting in reduced capacitance and conductance. Despite this reduction in the capacitance and conductance, tapered TPVs are still not electrically preferred, because such parasitic capacitance and conductance are not the dominant factors for TPVs in glass. It is attributed to the following three reasons.

1) Compared with TSVs, the capacitance and the conductance of TPVs in glass are smaller because of the low dielectric constant and the high resistivity of glass, and the via taper makes the capacitance and the conductance even smaller.

2) The impedance of GS TPVs at minimum pitch is calculated to be around 74 Ω, implying that the inductance is larger than the capacitance.

3) The sensitivity study of *S*-parameters on *RLCG* indicated that the resistance and the inductance of TPVs have a greater impact on the *S*-parameters than the conductance and capacitance do.

3.4 Analysis of Process Effect

This section discusses the effect of via metallization and fabrication on the electrical parameters. First, TPVs can be either fully plated or conformally plated, depending on the copper plating solution and processes. In addition, the via formation methods might induce sidewall roughness to enhance the copper adhesion to via sidewall. Finally, polymer liners might be formed around TPVs as a buffer layer to reduce the thermos-mechanical stress induced by mismatch in coefficient of thermal expansion

(CTE) between the copper and the glass. All of these process variations will have different impacts on the electrical performance of TPVs in glass, which will be in detail in this section.

3.4.1 Copper Plating

In practice, there are two via metallization methods: fully plating and conformal plating. The former is preferred electrically because TPVs are completely filled by the copper resulting in the lowest DC resistance values. Unfortunately, fully plating TPVs, especially those with larger diameters, is a slow process leading to higher cost. Hence, it is not favored for cost-sensitive applications. Conformally plated TPVs are preferred, even though they are higher DC resistance values. Moreover, as the frequency increases, the AC current is concentrated on the outer surface of the TPVs, which means that when the conformally-plated copper thickness is more than the skin depth, the AC resistance values of these TPVs are virtually equal to those of the fully-filled TPVs.

The effect of via metallization on the DC resistance was analyzed, because the DC resistance is more influenced by the conformal plating than the AC resistance. Although Equation 3.3 is derived for the AC resistance calculation of the fully-plated TPVs, it is applicable to calculate the DC resistance values of the conformally-plated TPVs just by replacing δ_s with the conformally-plated copper thickness t_m. In typical fabrication processes, the plated copper thickness is less than the minimum via radius which is the bottom radius for tapered TPVs. The relative difference of DC resistance values between the conformally-plated TPVs and the fully-plated ones can be calculated by (3.3) and (3.5) to obtain

$$\frac{\Delta R_{\text{TPV, DC}}}{R_{fully}} = \frac{R_{conf.} - R_{fully}}{R_{fully}}$$
$$= \frac{D \cdot \left(D - \frac{2 \cdot h}{\tan\theta} \right) \cdot \tan\theta \cdot \ln\left(1 - \frac{2}{\tan\theta} \cdot \frac{h}{D - t_m} \right)^{-1}}{8 \cdot h \cdot t_m} - 1 \quad . \tag{3.22}$$

When θ=90^o, this difference is

$$\left. \frac{\Delta R_{\text{TPV, DC}}}{R_{fully}} \right|_{90^o} = \frac{1}{4 \cdot (t_m / D) \cdot (1 - t_m / D)} - 1 . \tag{3.23}$$

Mathematically, the minimum value, i.e. zero in (3.23) occurs when t_m is equal to D/2. Intuitively, when TPVs are fully plated, which coincides with t_m = D/2, the DC resistance value is minimized. Yet, it is not the case for tapered TPVs in (3.22). Figure 3.11 presents the relative DC resistance difference computed by (3.22) for various conformally-plated copper thicknesses in the case of 30-μm-diameter tapered TPVs with 1.7 / 3.3 / 5.0 aspect ratios and 75^o / 80^o / 88^o taper angles. In fact, the via taper helps reduce the minimum copper thickness required in the conformal plating to ensure an adequate DC resistance close to the full plating. For example, the minimum copper thickness required in the conformal plating is about 4 μm to guarantee less than 10% DC resistance variation in the case of 30-μm-diameter TPVs with 1.7 aspect ratio and 75^o taper angle, 7 μm in the case of 30-μm-diameter TPVs with 1.7 aspect ratio and 80^o taper angle, as shown in Figure 3.11. The reason is that the more tapered TPVs have smaller radii at the bottom, and require less conformally-plated copper.

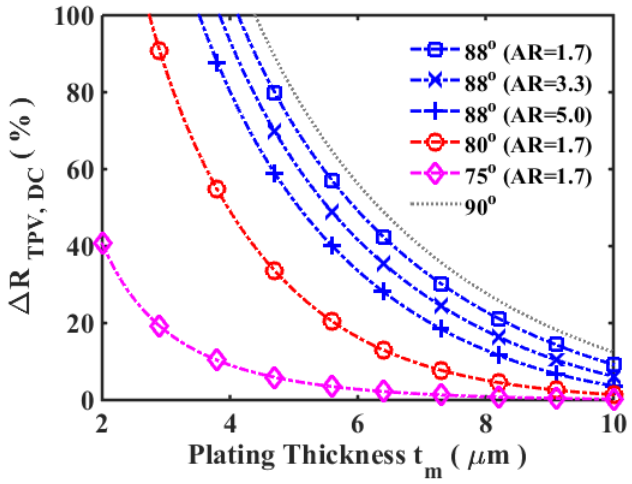
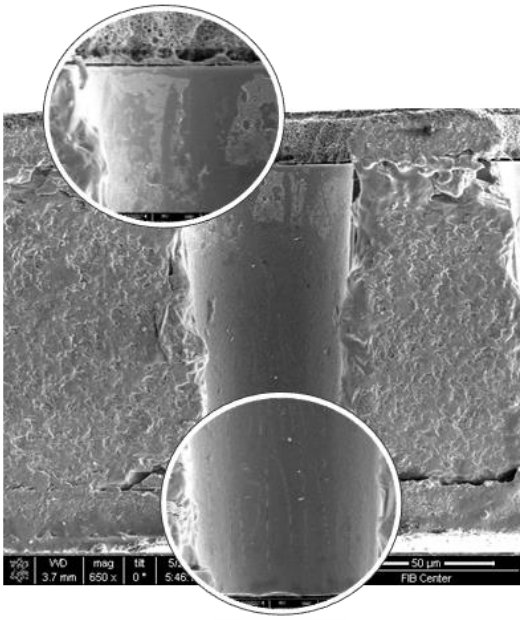


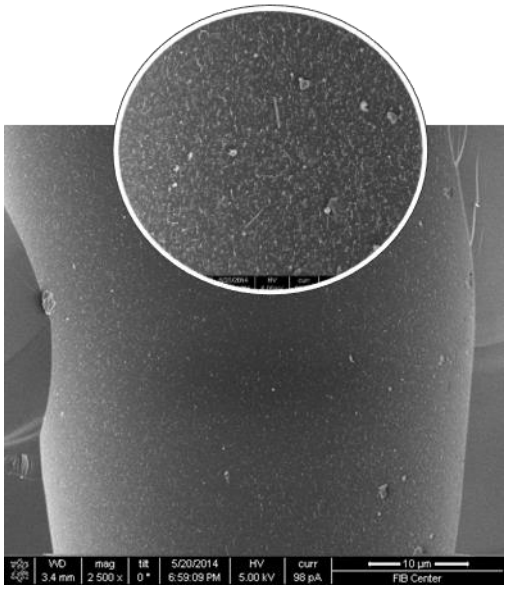
Figure 3.11: Relative difference of DC resistance in (14) with various conformally-plated copper thicknesses for 30-µm-diameter tapered TPVs with 1.7/3.3/5.0 aspect ratios and 75º/80º/88º taper angles.

3.4.2 Sidewall Roughness

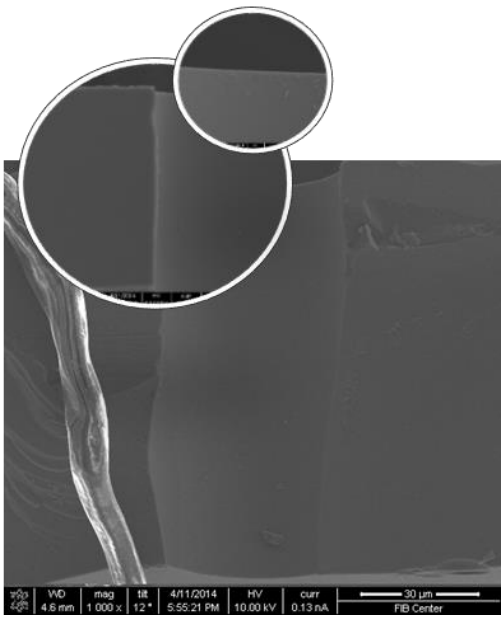
Depending on the TPV formation methods, via sidewalls have different amounts of surface roughness, which enhances copper adhesion to the via sidewall. However, the surface roughness would induce additional conductor loss to an ideally smooth conductor, especially when the average surface roughness is comparable to the skin depth. Even though the quantitative characterization of the via sidewall by atomic-force microscopy (AFM) is challenging because of the vertical nature of the via sidewall, a scanning electron microscope (SEM) characterization can provide qualitative information regarding via sidewall roughness. Based on the SEM images, reasonable estimations can be made for the average surface roughness values for TPVs formed by various methods.


WD
3.7 mm
mag
650 x
tilt
0 °
50 µm
FIB Center

(a)


WD
3.4 mm
mag
2 500 x
tilt
0 °
5/20/2014
6:59:09 PM
HV
5.00 kV
curr
98 pA
10 µm
FIB Center

(b)



(c)

Figure 3.12: SEM cross-section view of (a) a 60-µm TPV formed by ArF excimer laser ablation, (b) a 60-µm TPV formed by focused electrical-discharge method, and (c) a 30-µm TPV formed by the Corning method.

TPV formation methods accessible to the author include ArF excimer laser ablation, focused electrical-discharge method, and a proprietary glass via formation method developed by Corning Inc. Thus, one TPV formed by each method was randomly chosen and then observed using an SEM for the sidewall roughness estimation, with the SEM images presented in Figure 3.12.

The sidewall of TPVs formed by ArF excimer laser ablation had many polymer residues near the entrance side, where the laser ablation starts removing the material. The polymer residues originated from the polymer laminated on each side of the glass to enhance the copper adhesion to glass surface and also to prevent the glass from cracking during handling, and they can be removed by optimizing the laser ablation conditions. Thus, the polymer residues do not contribute to surface roughness. On the exit side, minor defects were observed because of the laser ablation, as shown in Figure 3.12 (a),

and the average surface roughness induced by these scratches is estimated to be 0.20 μm, which is consistent with the average surface roughness of vias formed by CO_2 laser [64].

The sidewall of TPVs formed by focused electrical-discharge method does not have polymer residues but tiny glass residues, as shown in Figure 3.12 (b). The bigger particles, which are about several micrometers in size, are glass debris that are left over from the diamond cutting to obtain the cross section, and should not be included in the analysis. Based on these qualitative observations, the sidewall of TPVs formed by focused electrical-discharge method is slightly better than the sidewall of TPVs formed by ArF excimer laser ablation, and the average surface roughness is estimated to be 0.10 μm, which is 100 times more roughened than that of the glass surface, typically in the 1-2 nm range [12].

Finally, the sidewall of TPVs formed by the Corning method was observed in commercially available EAGLE XG Slim^{TM} glass substrates provided by Corning Inc. [65, 66], while the detailed drilling method was not disclosed. It can be seen from Figure 3.12 (c) that the via sidewall is very smooth, and a small amount of debris is generated because of the diamond cutting during sample preparation. Therefore, a conservative estimation was made that the via sidewall is 10 times more roughened than the glass surface, which gives us an average surface roughness of 0.01 μm.

Thus, the average surface roughness for three different formation methods, namely ArF excimer laser ablation, focused electrical-discharge method, and the Corning drilling method, were estimated based on the qualitative SEM characterization of the via sidewalls. Since the average surface roughness for each TPV formation method is well below 2 μm, the Hammerstad model [60] can be used to account for the surface roughness in the conductor loss, and it is expressed as

$$R_{\mathrm{TPV,\,AC}}^{\mathrm{RMS}} = K_H \cdot R_{\mathrm{TPV,\,AC}} \tag{3.24}$$

where $R_{\mathrm{TPV,\,AC}}$ is calculated by equation (3.3), and K_H is the Hammerstad coefficient for a given average surface roughness. The formula for K_H is as follows,

$$K_H = 1 + \frac{2}{\pi} \cdot \arctan\left(1.4 \times \left(\frac{h_{\mathrm{RMS}}}{\delta_s}\right)\right) \tag{3.25}$$

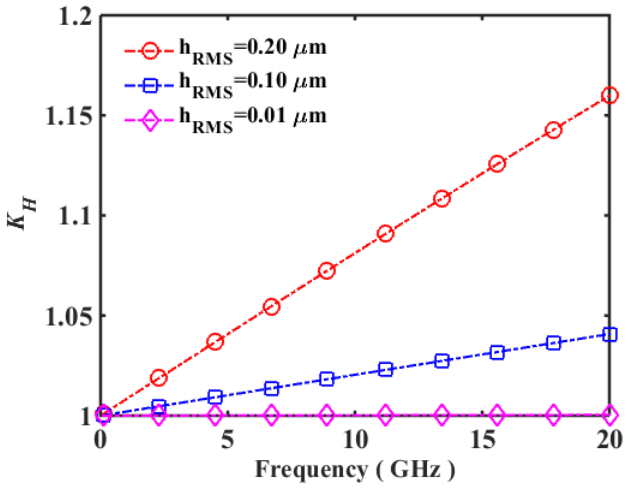
where h_{RMS} is the average value of the surface roughness, and δ_s is the skin depth at the operating frequency.

Substituting the value of the average surface roughness into equation (3.25) (h_{RMS}=0.20 μm for ArF excimer laser ablation, h_{RMS}=0.10 μm for focused electrical-discharge method, and h_{RMS}=0.01 μm for the Corning method), the Hammerstad coefficient can be calculated, as shown in Figure 3.13 (a). Since the skin depth of copper is greater than 0.40 μm across 0-20 GHz, the surface roughness for ArF excimer laser ablation increases the conductor loss up to 16% at 20 GHz, while the surface roughness for either focused electrical-discharge method or the Corning drilling method is not pronounced because the average surface roughness is still much less than the skin depth of copper at 20 GHz. Further analysis shows that for via sidewalls as smooth as that formed by focused electrical-discharge method, the surface roughness will not have a significant impact until 310 GHz; and for via sidewalls as smooth as that formed by the Coning method, the TPV sidewall roughness is negligible until 1 THz.

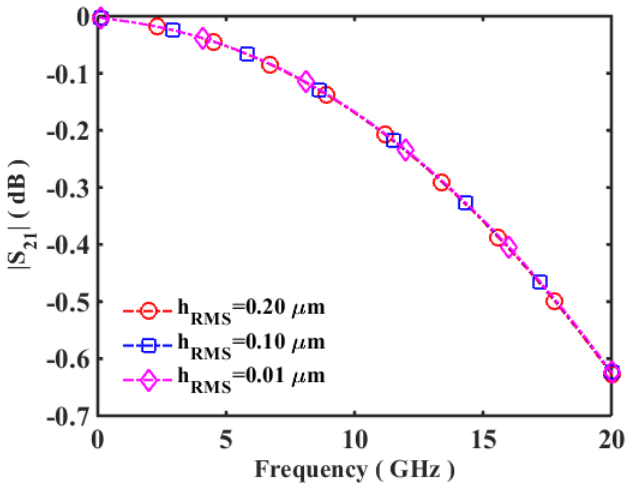
Then, S_{21} was computed using the circuit model proposed in Section 3.1 while taking via surface roughness into account. TPVs with 55 μm diameter and 88^{o} taper angle at 150-μm center-to-center pitch in 300-μm-thick glass were analyzed in this scenario. The calculated S_{21} magnitude is presented in Figure 3.13 (b) for TPVs formed by ArF excimer laser ablation, focused electrical-discharge method, and the Corning method. It can be seen that although the surface roughness varies for different TPV formation methods, its impact on the signal transmission is not significant. There are three reasons attributed to this: 1) the parasitic inductance and capacitance, especially the inductance, are dominant factors for the signal transmission, while the resistance comes third in the

order (see Subsection 3.2.4); 2) even though we conservatively assume that the via sidewall surface for ArF excimer laser ablation is close to the surface roughened by the desmear process in wet chemical plating, 0.4 μm average surface roughness is still relatively smooth, compared with the surface roughness in organic substrates; 3) the conductor loss increases with the square root of the frequency, while the substrate loss increases with the frequency, indicating that beyond a certain frequency, the conductor loss will be overwhelmed by the substrate loss.

Based on the aforementioned analysis, it can be concluded that the via sidewall surface is relatively smooth, and the surface roughness is not significant for signal transmission below 20 GHz.



(a)



(b)

Figure 3.13: (a) Calculated Hammerstad coefficients, and (b) calculated S_{21} magnitude based on the assumptions of average surface roughness to be 0.20 µm, 0.10 µm, and 0.01 µm, respectively for TPVs formed by ArF excimer laser ablation, focused electrical-discharge method, and the Corning method.

3.4.3 Polymer Liner

A liner is typically deposited as a barrier layer in TSVs to prevent copper from diffusing into silicon substrate and forming eutectics. The mechanical benefits of the polymer liner in TPVs in glass are twofold: 1) it acts as a stress buffer layer between the glass substrate and the copper; 2) it improves the adhesion of copper to via sidewall. However, the dielectric constant or the relative permittivity of polymer differs from that of glass, causing the capacitance variation for structures with and without polymer liner.

The conformal mapping method [38] was applied to a TPV pair with a signal and return TPVs. By doing so, the parallel TPV pair shown in Figure 3.14 (a) can be transformed to a parallel-plate geometry as shown in Figure 3.14 (b). Due to the symmetry of the TPV pair, only the right-sided TPV in Figure 3.14 (a) is described below. The circular interface between copper and polymer is expressed as

$$O_1 = p/2 + D_{Cu} \cdot e^{j\theta} \tag{3.26}$$

while the circular interface between polymer and glass is expressed as

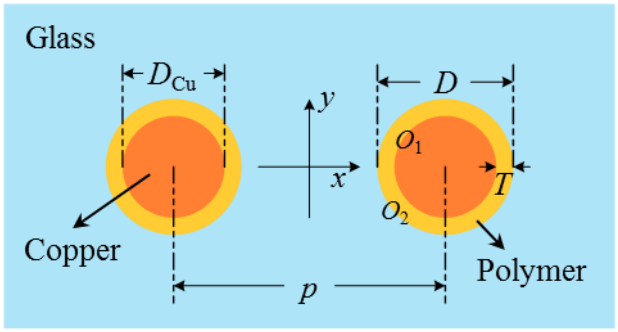
$$O_2 = p/2 + D \cdot e^{j\theta} \tag{3.27}$$

where D_{Cu} is the copper diameter, D is the glass via diameter, T is the polymer thickness, p is the center-to-center pitch between TPVs, as illustrated in Figure 3.14 (a), θ is the angle with respect to x-axis, and O_1 and O_2 are equal to $x_1+j\cdot y_1$ and $x_2+j\cdot y_2$, respectively.

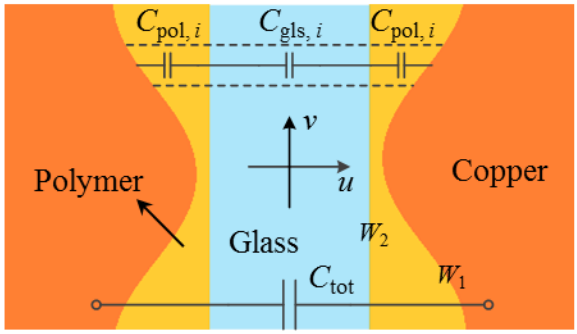
The mapping function used here is defined as

$$W_{1or2} = \ln \frac{O_{1or2} + q}{O_{1or2} - q} \tag{3.28}$$

where $2q = \sqrt{p^2 - D^2}$, and W_1 and W_2 are equal to $u_1+j\cdot v_1$ and $u_2+j\cdot v_2$, respectively. The top view of the mapped TPV pair is presented in u-v plane in Figure 3.14 (b), with the v-axis bounded within $-\pi$ and π. Therefore, using the conformal mapping, the circular interface between copper and polymer O_1 in x-y plane is transformed to the curved interface W_1 in u-v plane, while the circular interface between polymer and glass O_2 in x-y plane is transformed to the straight interface W_2 in u-v plane.



(a)



(b)

Figure 3.14: (a) Top view of a TPV pair in *x*-*y* plane, and (b) top view of the mapped TPV pair in *u*-*v* plane.

Similar to the method presented in Subsection 3.1.2 for computing the parasitic *RLCG*, the mapped parallel-plate geometry in Figure 3.14 (b) is divided into N strips along v-axis. For the ith strip, the per-unit-length polymer capacitance ($C_{\text{pol},i}$) and the per-unit-length glass capacitance ($C_{\text{gls},i}$) can be computed separately as

$$C_{\text{pol},i} = \varepsilon_0 \varepsilon_{\text{r, pol}} \frac{1 \times \Delta v_{1,i}}{\Delta u_{1,i}} = \varepsilon_0 \varepsilon_{\text{r, pol}} \frac{1 \times \left(v_{1,i+1} - v_{1,i}\right)}{\left(u_{2,i} - u_{1,i}\right)} \tag{3.29}$$

$$C_{\text{gls},i} = \varepsilon_0 \varepsilon_{\text{r, gls}} \frac{1 \times \Delta v_{2,i}}{2 \times u_{2,i}} = \varepsilon_0 \varepsilon_{\text{r, gls}} \frac{1 \times \left(v_{2,i+1} - v_{2,i}\right)}{2 \times u_{2,i}} \tag{3.30}$$

where ε_0 is the vacuum permittivity, and $\varepsilon_{\text{r, pol}}$ and $\varepsilon_{\text{r, gls}}$ are the dielectrc constants for the polymer and the glass, respectively.

Then, the per-unit-length total capacitance ($C_{\text{tot},i}$) for the ith strip is the combination of the per-unit-length glass capacitance ($C_{\text{gls},i}$) in series with two per-unit-length polymer capacitances ($C_{\text{pol},i}$), which is computed as

$$\frac{1}{C_{\text{tot},i}} = \frac{1}{C_{\text{gls},i}} + \frac{2}{C_{\text{pol},i}} \tag{3.31}$$

where $C_{\text{gls},i}$ and $C_{\text{pol},i}$ are computed by equation (3.29) and (3.30), respectively. Finally, the per-unit-length total capacitance (C_{tot}) for a TPV pair is the sum of N strips as follow

$$C_{\text{tot}} = \sum_{i=1}^{N} C_{\text{tot},i} \ . \tag{3.32}$$

It has been proved in [38] that as long as N is larger than 6, the computed results are close to those from full-wave simulation. Herein, we chose N to be 100 for the following study.

To study how the polymer liner affects the capacitance, the TPV pair without polymer liner was also considered by replacing the polymer line with glass in Figure 3.14 (a), and the effective dielectric constant is defined as

$$\varepsilon_{\text{eff}} = \frac{C_{\text{tot, w/ polymer}}}{C_{\text{tot, w/o polymer}}} \tag{3.33}$$

where $C_{\text{tot, w/ polymer}}$ is the per-unit-length total capacitance for a TPV pair with polymer liner, and $C_{\text{tot, w/o polymer}}$ is the per-unit-length total capacitance for a TPV pair without polymer liner.

TPVs of various diameters at various pitches were analyzed by this conformal mapping method and also were simulated by a 2-D EM solver [67]. Specifically, TPV diameters were varied as 18 μm, 30 μm and 60 μm, and TPV pitches were varied from $2.5 \cdot D$ up to $6 \cdot D$. Also, the dielectric constants of polymer and glass in this analysis are 3.26 and 5.3, respectively. In Figure 3.15, the effective dielectric constants computed by the conformal mapping method and simulated by the 2-D EM solver are presented for 18-/30-/60-μm-diameter TPVs at various pitches.

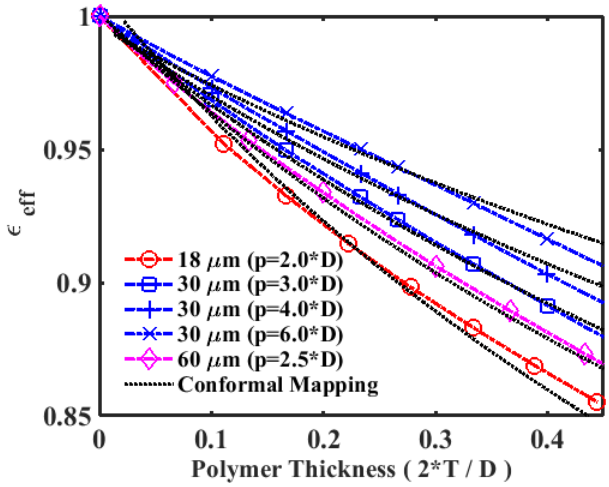


Figure 3.15: Effective dielectric constants computed by the conformal mapping method and simulated by the 2-D EM solver for 18-/30-/60-μm-diameter TPVs at various pitches.

It can be seen that the effective dielectric constants computed by the conformal mapping method match those calculated by the 2-D EM solver, with the maximum error less than 1%, which in turn validates the feasibility and accuracy of this method. In addition, it is found that as the thickness of polymer liner increases to a quarter of glass via diameter, the effective dielectric constant decreases to as much as 0.84, and as the pitch increases, the decreasing rate of the effective dielectric constant flattens out. This can be explained as follows: with the increasing thickness of the polymer liner, there is more polymer instead of glass between the parallel copper plate in the *u*-*v* plane, and the dielectric constant of polymer is lower than that of glass, resulting in lower effective dielectric constant; with the pitch increasing, the parallel copper plate is separated further, and the volume of glass is much more than that of polymer, making the polymer liner less significant to the effective dielectric constant.

3.5 Nonlinearly Tapered TPVs

The proposed circuit model in Section 3.1 is based on the assumption that TPVs in glass are linearly tapered, as shown in Figure 3.1 (a). However, the via shapes for some drilling methods do not exactly follow this assumption, including TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method. It is of interest to consider nonlinearly tapered TPVs formed by these methods. In this section, a computer-aided approach is proposed to fit the nonlinear via shape and to compute the parasitic resistance (R), loop inductance (L), capacitance (C), and conductance (G).

3.5.1 Proposed Computation Scheme

To analyze nonlinearly tapered TPVs, a computer-aided approach was proposed to compute the *RLCG* parasitics of such TPVs. The flow chart of this approach is presented in Figure 3.16. First, the nonlinearly tapered TPVs have to be cross-sectioned and then observed using an optical microscope or an SEM. During observation, at least four sets of data points need to be measured as the via radius at the vertical position above the bottom of glass to determine the via shape. The more data points that are collected, the better accuracy of the via shape approximation. It is also recommended that these data points are chosen to be at positions where the via shape changes significantly. Based on these measured data points, the [68] was used to fit the nonlinear via shape. Figure 3.17 presents the SEM image of a nonlinearly tapered TPV formed by the focused electrical discharge method and the fitted via shape by the shape-preserving piecewise cubic interpolation. In this example, five data points were collected with one at the bottom, one on the top, and the other three distributed at the vertical positions around 13 μm, 40 μm, and 80 μm from the bottom.

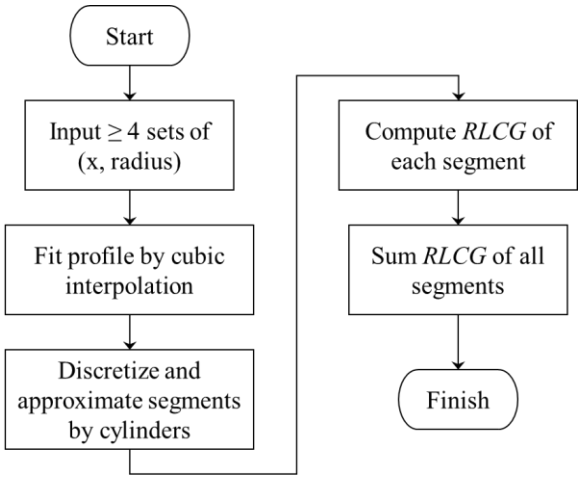


Figure 3.16: Flow chart to compute *RLCG* for nonlinearly tapered TPVs.

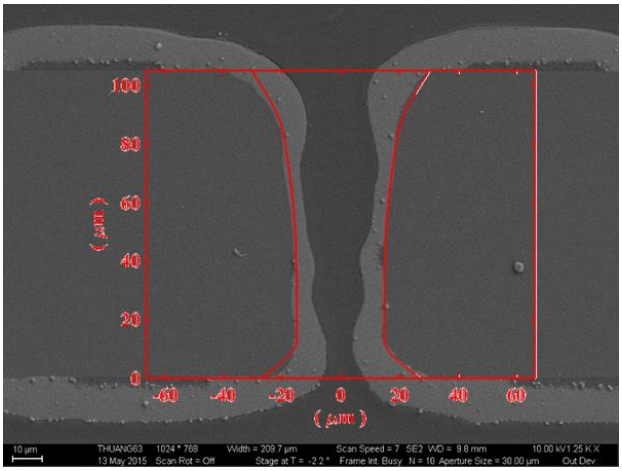


Figure 3.17: SEM image of a nonlinearly tapered TPV formed by the focused electrical discharge method and the fitted via shape by the shape-preserving piecewise cubic interpolation.

After obtaining the via shape, the idea presented in Subsection 3.1.2, that is, to slice TPVs horizontally into many cylindrical pieces, can be used for the analysis of nonlinearly tapered TPVs. The *RLCG* values for each cylindrical piece are computed using the transmission-line parameters for parallel wires. Then, summing up *RLCG*

values for each cylindrical piece gives the total *RLCG* values for the nonlinearly tapered TPVs, which concludes the analysis of nonlinearly tapered TPVs.

3.5.2 Discussion

Based on the proposed approach, nonlinearly tapered TPVs, formed by the previously-reported TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method, were analyzed and compared in terms of parasitic resistance, loop inductance, capacitance, and conductance. The via shapes for these methods are the same as those presented in Section 1.2 in CHAPTER 1. As the prior arts of drilling TPVs by these methods focus on different glass thicknesses and via diameters, the parasitic *RLCG* values are normalized before comparison for each of these drilling methods. Since the resistance is proportional to the length but inversely proportional to the cross-section area, the resistance values are normalized as

$$R_N = R_{\text{TPV}} \times \left(\frac{\pi}{4} D^2 \right) \Big/ h \tag{3.34}$$

where R_{TPV} is either DC or AC resistance computed by the proposed approach, D is the maximum diameter along via length, and h is the via length. The values for loop inductance, capacitance, and conductance are normalized only by the via length as

$$L_N = L_{\text{TPV}} / h \tag{3.35}$$

$$C_N = C_{\text{TPV}} / h \tag{3.36}$$

$$G_N = G_{\text{TPV}} / h \tag{3.37}$$

where L_{TPV}, C_{TPV}, G_{TPV} are the computed loop inductance, capacitance, and conductance by the proposed approach, respectively.

The normalized DC resistance and the normalized 1 GHz resistance are compared in Figure 3.18 for TPVs formed by the TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method. It is found that TPVs formed by the CO_2 laser and TiSa laser have the largest normalized DC and 1 GHz resistance,

respectively; and TPVs formed by the focused electrical discharge method have the smallest normalized resistances.

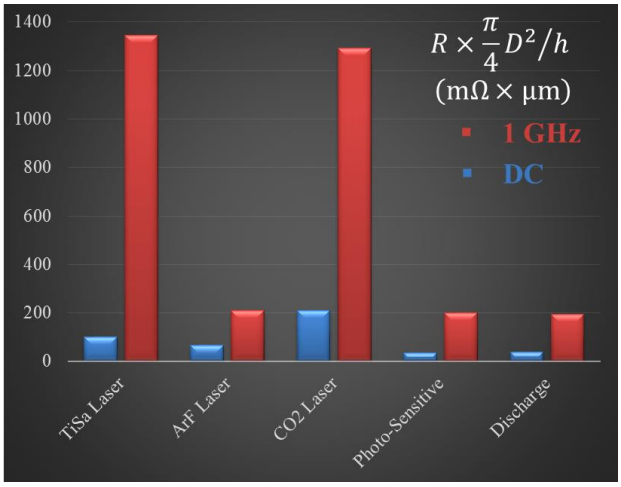


Figure 3.18: Comparison of DC and 1 GHz resistance for TPVs formed by the TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method.

Next, the normalized loop inductance is compared in Figure 3.19. It is assumed that TPVs are placed at a minimum pitch ($p = 2D$) for the purpose of computation, even though the maximum diameter is 277 μm for TiSa laser, 50 μm for ArF laser, 120 μm for CO_2 laser, 66 μm for photo-sensitive method, and 60 μm for focused electrical discharge method. From Figure 3.19, it can be seen that TPVs formed by CO_2 laser have the highest normalized loop inductance, and TPVs formed by the photo-sensitive method and also by the focused electrical discharge method have the smallest normalized loop inductance.

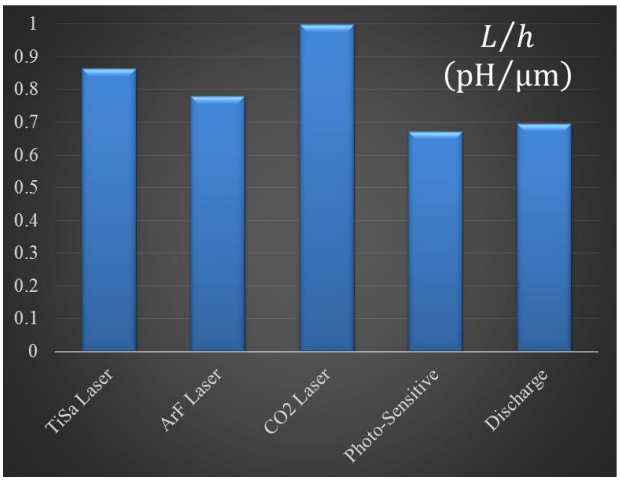
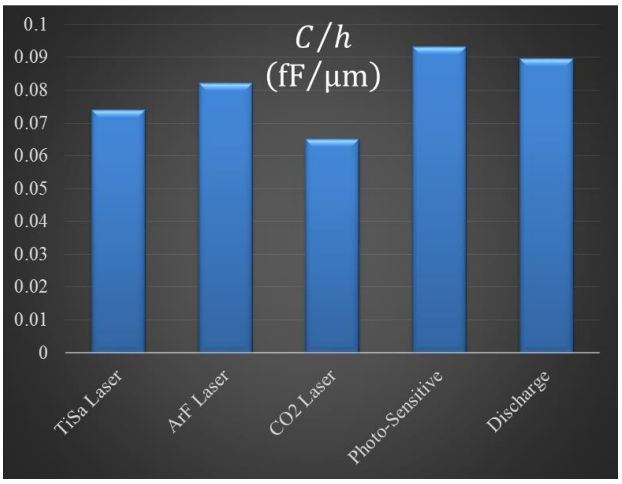
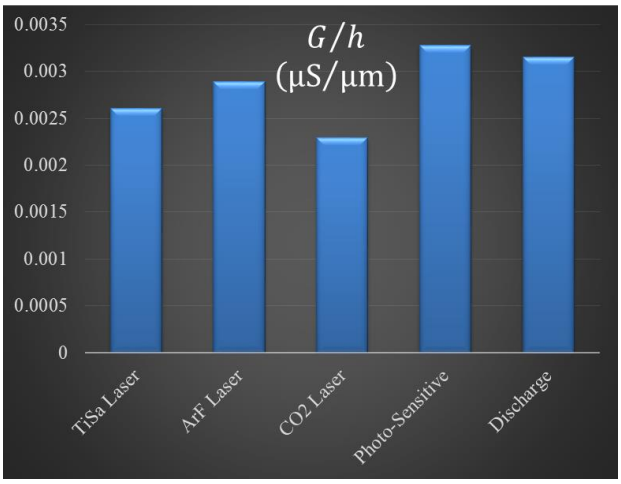


Figure 3.19: Comparison of loop inductance for TPVs formed by TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method.

Finally, the normalized capacitance and conductance at 1 GHz are compared in Figure 3.20, based on the assumption that TPVs are placed at the minimum pitch ($p = 2D$), as well. It is found that TPVs formed by the photo-sensitive method have a higher normalized capacitance and conductance than those formed by other methods.



(a)



(b)

Figure 3.20: Comparison of (a) capacitance and (b) conductance for TPVs formed by the TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method.

Overall, TPVs formed by ArF laser, photo-sensitive method, and focused electrical discharge method have better electrical performance than those formed by TiSa laser and CO_2 laser. However, except the normalized resistance, the normalized loop inductance, capacitance, and conductance, are just slightly better. It is important to note that the scalability and via formation speed of these methods are very important for the fabrication of glass interposers, but they are not compared here as they are beyond the scope of this dissertation.

3.6 Summary

1) New Circuit Model: TPVs in glass have a tapered shape, and a wideband scalable circuit was proposed in this chapter to model such tapered TPVs, with analytical or semi-analytical equations derived for the *RLCG* parameters in the proposed model. The convergence study shows that as long as tapered TPVs are sliced by more than 10 pieces, the convergence error is less than 10%. The *S*-parameters computed from the proposed

model were compared with those from the 3D EM solver, and the maximum difference of S_{21} magnitude is 0.01 dB, while that of S_{21} phase is 1 deg. Furthermore, the proposed model was found to be in excellent agreement with that of the measurement with maximum error for S_{21} magnitude and phase about 0.05 dB and 2° below 20 GHz, respectively. The sensitivity studies show that the parasitic inductance, capacitance, resistance, and conductance have the first, second, third, and fourth most pronounced impacts on *S*-parameters, respectively.

2) Taper Effect: The effect of via taper on the *RLCG* parameters was investigated. It was found that the parasitic capacitance and conductance values for tapered TPVs were 40% lower than those for straight ones. The adverse effect of via taper is that it increases the via resistance and the inductance, which are the dominant factors for TPVs in glass substrates. The AC resistance was proved to be less influenced by the taper than the DC resistance, and the maximum inductance increase is about 80%.

3) Process Effect: The effects of copper plating, sidewall roughness, and polymer liner were studied in terms of different electrical parameters. The analysis of copper plating shows that the via taper helps reduce the minimum copper thickness required in the conformal plating to ensure an adequate DC resistance close to that of the full plating. Based on the observation of via sidewall through SEM for TPVs formed by ArF excimer laser, focused electrical-discharge method, and the Corning drilling method, as well as the analysis through Hammerstad model, the following have found: 1) the surface roughness for ArF excimer laser ablation increases the conductor loss up to 16% at 20 GHz; 2) the surface roughness for focused electrical-discharge method does not have a significant impact up to 310 GHz; 3) the surface roughness for the Corning drilling method remains negligible up to 1 THz. Finally, the effect of polymer liner was studied by conformal mapping method and results show that as the thickness of polymer liner increases to a quarter of the glass via diameter, the effective dielectric constant decreases

to as much as 0.84, and as the pitch increases, the decreasing rate of the effective dielectric constant flattens out.

4) Nonlinear Taper: A computer-aided approach was proposed to analyze nonlinearly tapered TPVs formed by TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method. Based on the observations through optical microscope or SEM, nonlinearly tapered via shapes were approximated by the shape-preserving piecewise cubic interpolation, and the *RLCG* of such TPVs were computed. The results show that TPVs formed by ArF laser, photo-sensitive method, and focused electrical discharge method have better performance than those formed by TiSa laser and CO_2 laser, but the difference between their performance is not that significant.

CHAPTER 4

DESIGN OF TAPERED TPVS FOR SIGNAL INTEGRITY

This chapter discusses the design of tapered TPVs in glass interposers for improved signal integrity in terms of signal transition, impedance discontinuity, and crosstalk.

The first task was to study the *S*-parameters of TPVs with various taper angles, and the results indicate that signals transiting through TPVs suffer less than a 1 dB loss. The effect of via taper on the time-domain eye diagrams was also investigated, and it was concluded that while the eye diagrams of TSVs in silicon interposers were noticeably degenerated, TPVs in glass interposers did not have a significant impact on the eye diagrams.

The second task was to analyze the TPV-induced impedance discontinuity using time-domain reflectometry (TDR), and the results indicated that the impedance variation exceeded the design target (≤5%). As a result, design techniques were proposed and demonstrated to minimize such impedance discontinuity by inserting additional ground TPVs to increase the via capacitance.

Finally, the basic Ground-Signal-Ground (GSG) TPV crosstalk structures were modeled by an equivalent circuit that was verified against both 3D EM simulations and measurements. Two worst cases with two aggressors and four aggressors were analyzed in the time domain, with the coupling noises larger than the design target of -30 dB. Therefore, five techniques were proposed and studied to suppress the crosstalk noise.

4.1 Signal Transition

One of the primary functions for TPVs in glass is to provide seamless signal transitions between different metal layers. However, due to the parasitics discussed in

CHAPTER 3, the electrical signals might be distorted. This section discusses the overall electrical performance of TPVs in glass, with the taper effect taken into account, and the analysis is carried out using the frequency-domain *S*-parameters and the time-domain eye diagrams.

4.1.1 *S*-Parameters

The basic structure of a TPV pair consisting of a signal TPV and a return or ground TPV, as shown in Figure 4.1, was studied. TPVs in this Ground-Signal (GS) configuration have a 30-μm diameter at a minimum 60-μm center-to-center pitch. The aspect ratios (ARs) were varied as 1.7, 3.3, and 5.0, and for the AR of 1.7, the taper angles were varied as 75º, 80º, and 88º. The excitation port 1 is placed on the top of TPVs, while the excitation port 2 is placed at the bottom of TPVs. Both excitation ports have a 50 Ω impedance. The glass substrate used for the simulations has a dielectric constant of 5.3 and a loss tangent of 0.006 at 10 GHz, while the annealed copper has a conductivity of 5.8×10^7 S·m.

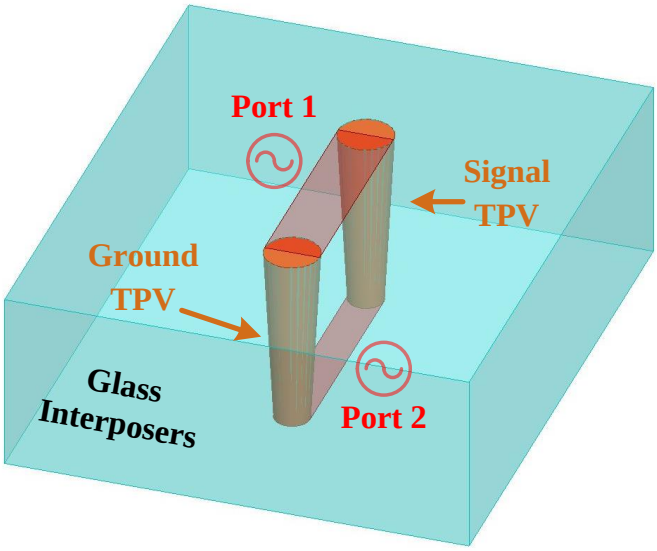
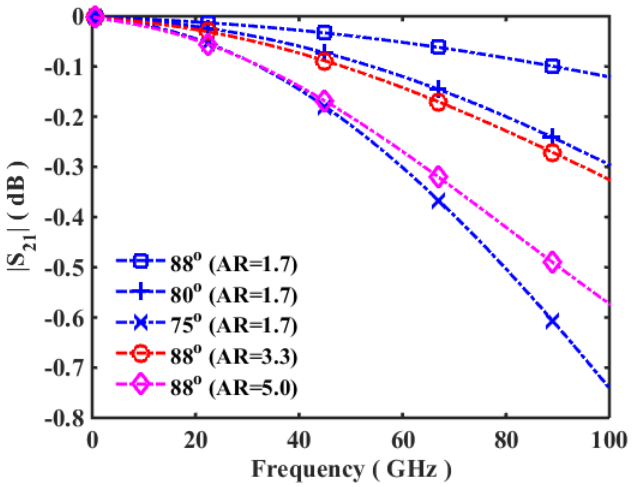


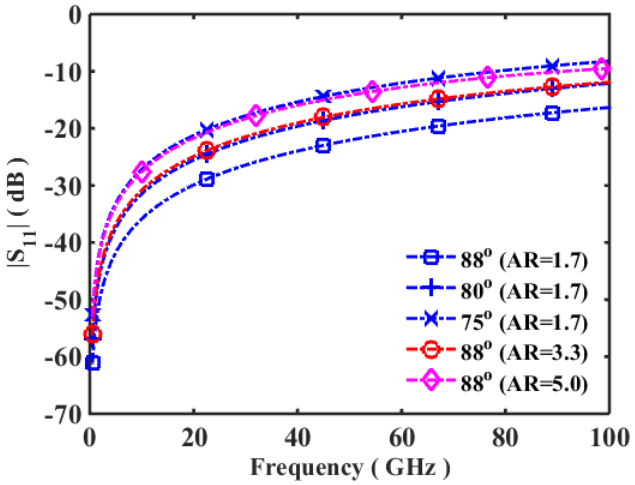
Figure 4.1: Structure of a TPV pair consisting of a signal TPV and a return or ground TPV used for the simulations.

The various TPV structures based on Figure 4.1 were simulated across 0.1 - 100 GHz using a 3-D EM solver — high frequency structural simulator (ANSYS HFSS) [67]. The simulated S_{21} and S_{11} magnitudes are plotted in Figure 4.2. The S_{21} magnitude indicates the amount of the energy transmitted from port 1 to port 2 while port 2 is match terminated. Three conclusions can be drawn from Figure 4.2 (a): 1) S_{21} magnitude decreases with increasing frequency, because the total loss including conductor loss, substrate loss, reflection loss, and radiation loss, increases as frequency increases; 2) for a given AR, S_{21} magnitude decreases with decreasing taper angles, because the via taper decreases the volume of copper inside TPVs, while increasing the reflection loss; 3) for a given taper angle, S_{21} magnitude decreases with increasing AR, because the via length increases with increasing AR, resulting in higher conductor, substrate, and reflection losses.

The S_{11} magnitude indicates the amount of the energy reflected back to port 1, when the signal is sent from port 1, and port 2 is match terminated. Essentially, it is related to the reflection loss. It can be seen from Figure 4.2 (b) that the S_{11} magnitude increases with increasing frequency, decreasing taper angle, and increasing AR.



(a)



(b)

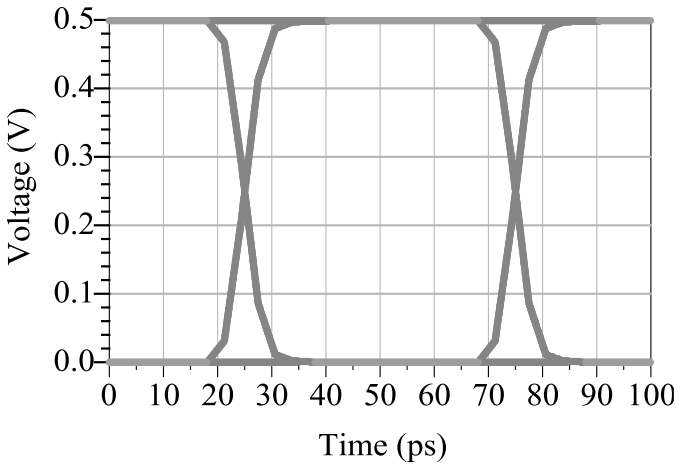
Figure 4.2: Simulated (a) S_{21} magnitude and (b) S_{11} magnitude of 30-µm-diameter tapered TPVs with 1.7/3.3/5.0 ARs and 75°/80°/88° taper angles at minimum pitch.

In conclusion, via taper has negative effects on the *S*-parameters, and as the aspect ratio increases, these negative effects are exacerbated. However, it is important to note from Figure 4.2 (a) that even for TPVs with the worst taper angle (75°) at 100 GHz, the S_{21} magnitude is still greater than -1 dB (90%), indicating that signal transitions through TPVs in glass will not suffer severe distortion.

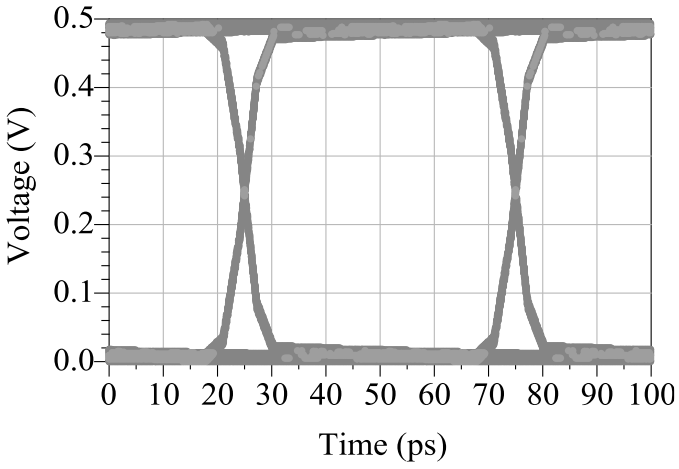
4.1.2 Eye Diagram

Based on the frequency-domain *S*-parameters, eye-diagram simulations were conducted to analyze the time-domain degeneration for signals transiting through TPVs. The time-domain pseudo-random bit sequence had a length of 2^{10}-1, with a 5-ps rise-and-fall time. The bit rate was set to 20 Gbps, and the source impedance was set to 50 Ω. The high-level voltage was 1 V, while the low-level voltage was 0 V. Each bit was sent at the top of TPVs and recorded at the bottom of TPVs to generate eye diagrams. The simulated eye diagrams of 30-µm TPVs in 150-µm glass interposers are shown in Figure 4.3 (a), and those of 30-µm TSVs in 150-µm silicon interposers are shown in Figure 4.3 (b) for

comparison. It can be seen from Figure 4.3 that both eye diagrams are widely open, because the test structures include only the TPVs or TSVs. Compared with TSVs in silicon, TPVs in glass have better eye opening, primarily due to the low substrate loss in glass.



(a)



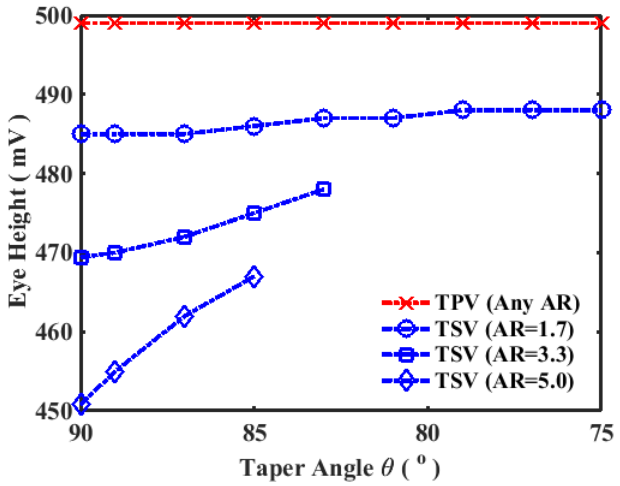
(b)

Figure 4.3: Simulated eye diagrams of (a) TPVs in glass interposers and (b) TSVs in silicon interposers at a bit rate of 20 Gbps.

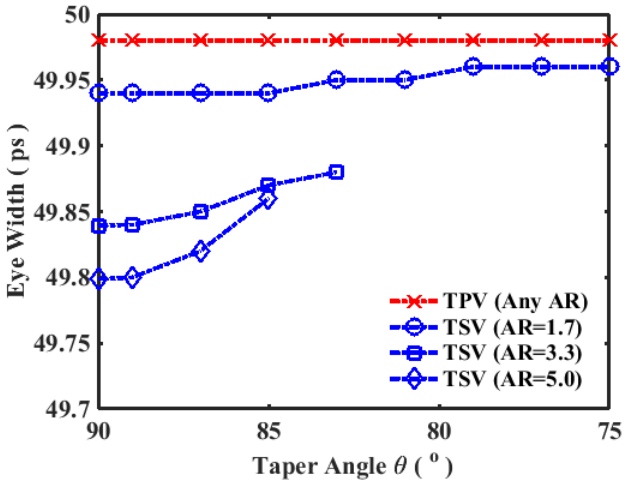
To quantify the effect of via taper on the eye diagrams, the taper angles were varied from 75^{o} to 90^{o}, and the aspect ratios were varied as 1.7, 3.0, and 5.0. In addition

to TPVs in glass interposers, TSVs in silicon interposers were also investigated in this study for comparison.

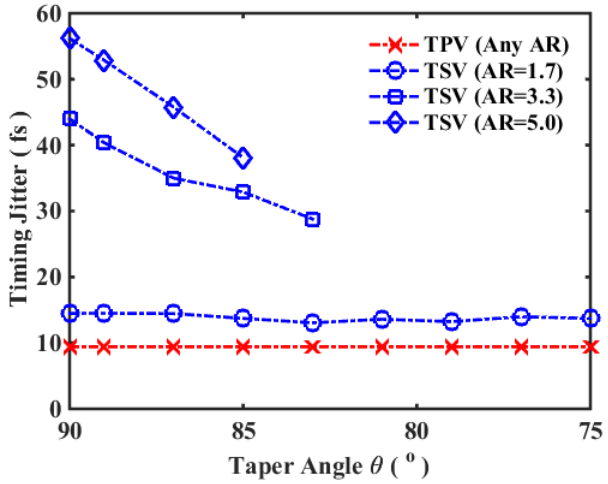
The effect of via taper on the eye height, eye width, and timing jitter is shown in Figure 4.4 (a), (b), and (c), respectively. From the results shown in Figure 4.4, it can be seen that for TPVs of different ARs in the glass interposer, the eye height, eye width, and timing jitter remain almost constant for all taper angles. The values of the eye height, eye width, and timing jitter are 499 mV, 49.98 ps, and 9.43 fs (0.019% of one unit interval), respectively. The reason why the eye-diagram parameters are not significantly affected by the taper angles is that the decrease of S_{21} magnitude shown in Figure 4.2 does not exceed 10%, and most of the high-frequency harmonics in the spectrum do not suffer much attenuation and delay.



(a)



(b)



(c)

Figure 4.4: (a) Eye height values, (b) eye width values, and (c) timing jitter values vary with taper angles for 30-µm-diameter vias with 1.7/3.3/5.0 ARs in glass and silicon interposers.

Unlike TPVs in glass, even one signal transition though TSVs in silicon causes noticeable eye-diagram degeneration, as shown in Figure 4.4: the eye-height reduction can be as much as 50 mV; the eye-width reduction can be as much as 0.2 ps; the timing jitter degeneration can be as much as 56.19 fs (0.11% of one unit interval). In addition, it

is found that the via taper improves the eye diagram of TSVs in silicon interposers, and the improvement of the eye height, eye width, and timing jitter can be as much as 3.59%, 0.12%, and 32.19%, respectively.

Therefore, while signal transition through TSVs in silicon interposers suffers noticeable degeneration and the taper improves the eye diagrams, TPVs in glass interposers are almost electrically transparent and the taper has no significant impact on the eye diagrams.

4.2 Impedance Discontinuity

As identified in CHAPTER 1, one of the challenges for TPV design is the impedance discontinuity: when the incident signal travelling along RDLs reaches the electrical interface between RDL and TPVs, it encounters a different impedance of TPVs, resulting in reflection which degenerates the signal transition through TPVs and might be the source of electromagnetic interference (EMI). In this Section, such a TPV-induced impedance discontinuity was first analyzed through time-domain reflectometry (TDR), and then design techniques were proposed to minimize the impedance discontinuity.

4.2.1 TDR Analysis

The structure used for TDR analysis is similar to the one in Figure 4.1 for *S*-parameter and eye-diagram analysis, as illustrated in Figure 4.5. Instead of two excitation ports, a voltage source generating the step waveform and a 50 Ω source impedance is placed on the top of the GS TPV pair, and a 50 Ω termination is placed at the bottom. The step waveform was set up to rise from 0 V to 1 V within 15 ps, and it was delayed by 15 ps in time. It is assumed that the impedances of RDL on the top and bottom are designed for 50 Ω match.

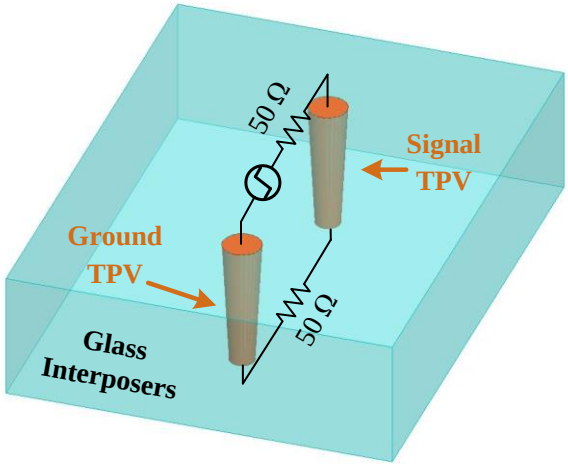


Figure 4.5: Structure for TDR analysis: a TPV pair with a voltage source having the step waveform and a 50 Ω source impedance on the top and a 50 Ω termination at the bottom.

The scenarios used in Sub-Section 4.1.1 were also used here, and the simulated TDR responses are plotted in Figure 4.6. The TDR responses indicate that there is an inductive discontinuity due to TPVs. In addition, as the taper angles decrease and the aspect ratios increase, the maximum impedance in the TDR response increases.

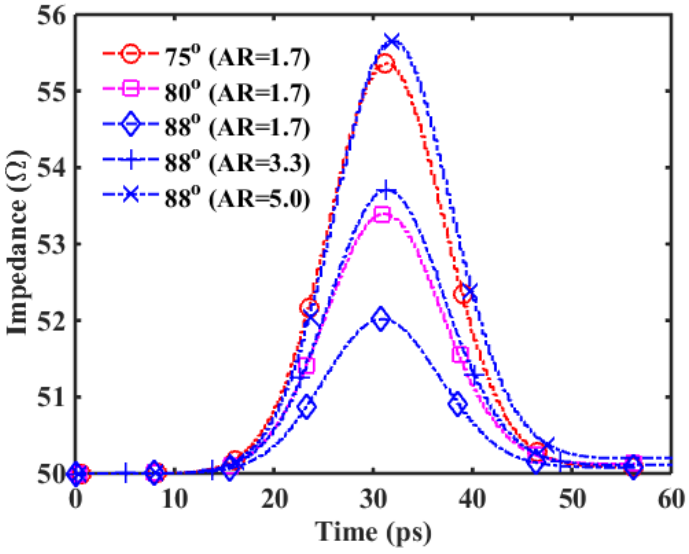
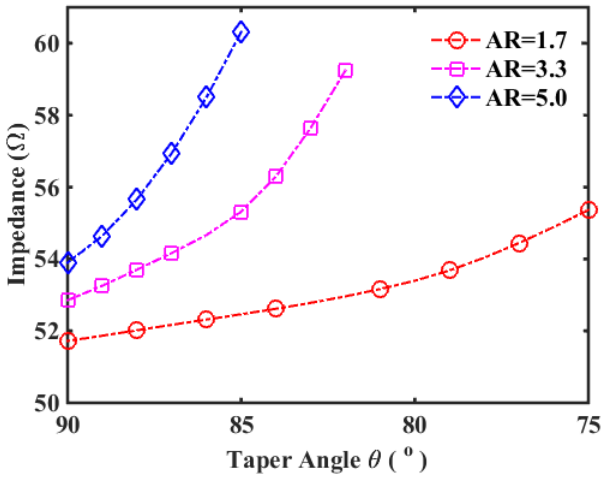
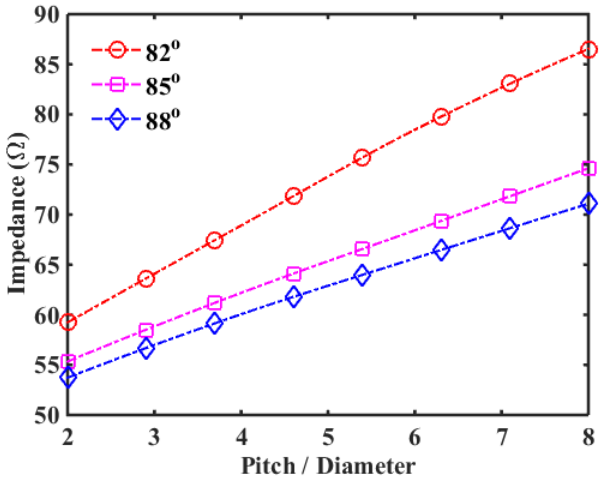


Figure 4.6: Simulated TDR responses for 30-µm-diameter tapered TPVs with 1.7/3.3/5.0 ARs and 75°/80°/88° taper angles at minimum pitch.

Then, the TDR responses were studied on 30-μm-diameter TPVs with various taper angles and pitches. The maximum impedances in these simulated TDR responses are plotted in Figure 4.7 (a) and (b), respectively. It is found from Figure 4.7 (a) that for 30-μm-diameter TPVs with 5.0 AR and 85^{o} taper angle at minimum pitch, the maximum impedance increases to 60.31 Ω, corresponding to +20.62% impedance discontinuity induced by TPVs. Based on Figure 4.7 (b), it is found that the maximum impedances in the simulated TDR responses increase with increasing pitches. For 30-μm-diameter tapered TPVs with 3.3 AR and 82° taper angle, the maximum impedance increases from 59.24 Ω to 86.52 Ω, as the ratio of pitch to diameter increases from 2 to 8.



(a)



(b)

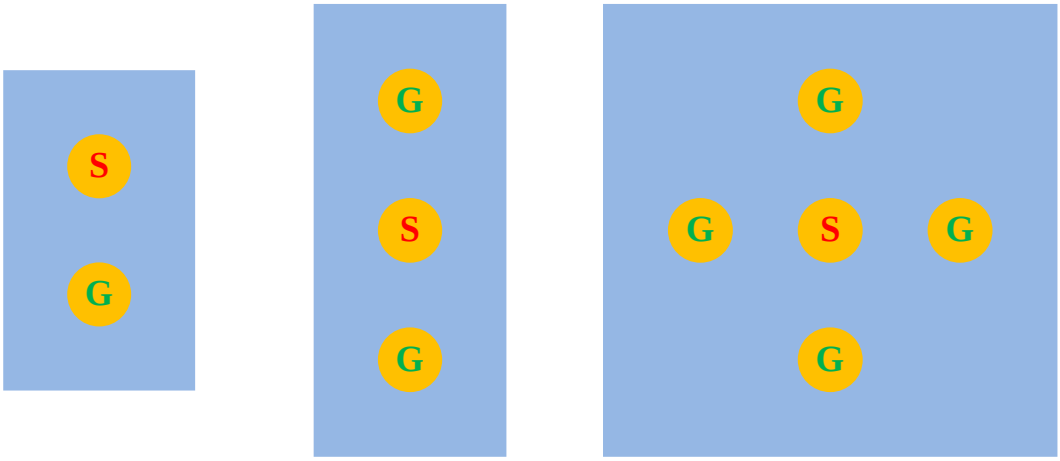
Figure 4.7: Maximum impedances in simulated TDR responses (a) for 30-µm-diameter tapered TPVs with 1.7/3.3/5.0 ARs and various taper angles at minimum pitch, and (b) for 30-µm-diameter tapered TPVs with 3.3 AR and 82°/85°/88° taper angles at various pitches.

The reason why the maximum impedance in the simulated TDR responses increases with decreasing taper angles and increasing via pitches is that decreasing taper angles and increasing via pitches cause the via inductance to increase but the via capacitance to decrease. The characteristic impedance is proportional to the square root of inductance but inversely proportional to the square root of capacitance. Hence, the characteristic impedance of TPVs increases, resulting in stronger inductive discontinuity and larger value of maximum impedance in the simulated TDR responses.

4.2.2 Minimization Techniques

The TDR responses presented in Sub-Section 4.1.1 indicate an inductive discontinuity due to tapered TPVs. To minimize such an impedance discontinuity, three via configurations shown in Figure 4.8 were compared using TDR analysis. Figure 4.8 (a) shows the GS via configuration as the reference, and Figure 4.8 (b) and (c) show the

proposed GSG and G4S1 via configurations, respectively, to minimize the impedance discontinuity.

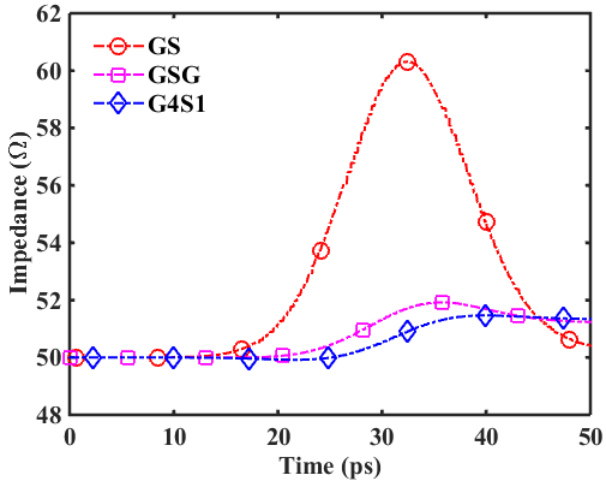


(a) (b) (c)

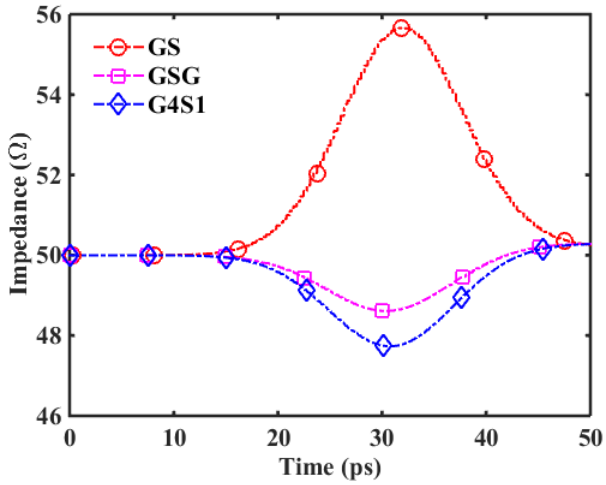
Figure 4.8: Top view of three via configurations to minimize impedance discontinuity: (a) GS TPVs; (b) GSG TPVs; (c) four ground TPVs with a signal TPV (G4S1).

Essentially, GSG and G4S1 via configurations are to insert additional ground TPVs around a signal TPV to increase the via capacitance and consequently to decrease the characteristic impedance. For 30-μm-diameter TPVs with 5.0 AR and 85° taper angle at minimum pitch, the simulated TDR responses of GS, GSG, and G4S1 configurations are plotted in Figure 4.9 (a). The maximum impedance in the simulated TDR response is 60.31 Ω for the GS configuration, 51.92 Ω for the GSG configuration and 51.47 Ω for the G4S1 configuration, bringing the impedance discontinuity within the 5% target tolerance. Similarly, the simulated TDR responses for 88° tapered TPVs are plotted in Figure 4.9 (b), and the maximum impedances are 55.66 Ω, 48.61 Ω, and 47.73 Ω, for GS, GSG, and G4S1, respectively. Thus, rather than assigning one ground or return TPV to a signal TPV, i.e. GS configuration, inserting multiple ground TPVs around a signal TPV can

bring down the characteristic impedance, leading to less inductive discontinuity due to tapered TPVs in glass interposers.



(a)



(b)

Figure 4.9: Simulated TDR responses for 30-µm-diameter tapered TPVs of GS, GSG, and G4S1 configurations with 5.0 AR and (a) 85°/ (b) 88° taper angles at minimum pitch.

Finally, the following three conclusions can be drawn for this section: 1) signal transition through tapered TPVs in glass interposers suffers inductive discontinuity; 2)

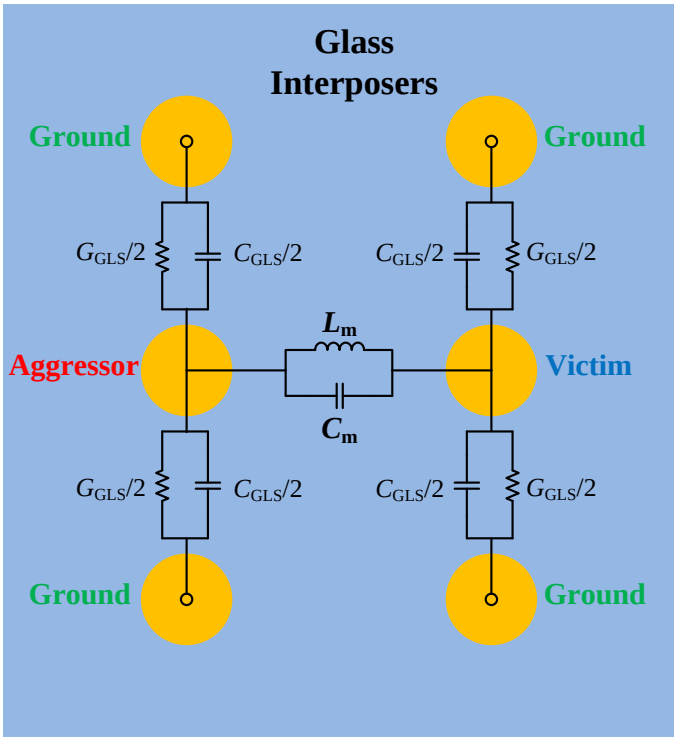
the maximum impedance in the TDR response increases with decreasing taper angles, increasing aspect ratios, and increasing via pitches; 3) inserting multiple ground TPVs around a signal TPV by using GSG or G4S1 configurations can minimize the impedance discontinuity.

4.3 Crosstalk

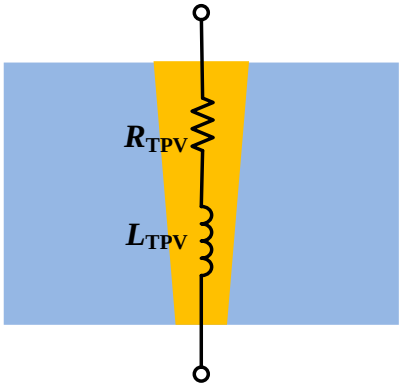
In practice, TPVs in glass interposers are placed in close proximity to each other to enable high interconnection density. Thus, when a TPV is active in sending signals, called an aggressor, an inactive TPV, called a victim, might be affected by crosstalk noise coupled from the aggressor. This section studies the basic GSG-to-GSG TPV crosstalk and two worst cases with two aggressors and four aggressors. Then, five techniques were proposed and investigated to suppress crosstalk between TPVs.

4.3.1 Multiple-TPV Scheme

Figure 4.10 (a) shows the top view of the GSG-to-GSV TPV structure for crosstalk analysis. The GSG TPVs on the left contain the aggressor TPV, while the GSG TPVs on the right contain the victim TPV. For both the aggressor TPV and the victim TPV, there is a capacitor (C_{GLS}) and a conductor (G_{GLS}) in shunt through glass to the ground TPVs. In addition, a mutual inductor (L_m) and a mutual capacitor (C_m) in shunt exist between the aggressor TPV and the victim TPV, which model the inductive and capacitive coupling between them. Each TPV is also modelled as a resistor (R_{TPV}) in series with a self-inductor (L_{TPV}), as shown in Figure 4.10 (b).



(a)



(b)

Figure 4.10: (a) Top view of the GSG-to-GSV TPV structure for crosstalk analysis and the equivalent circuit model with the capacitance (C_{GLS}) and conductance (G_{GLS}) through glass and the mutual inductance (L_m) and mutual capacitance (C_m); (b) cross-section view of a single TPV in the GSG-to-GSV TPV structure and its equivalent circuit model with the via resistance (R_{TPV}) and self-inductance (L_{TPV}).

Before further analysis, the TPV noise coupling from the equivalent circuit model was verified against 3D EM simulations and measurements in the frequency domain. Two GSG-to-GSG coupling structures with different coupling strengths were designed, simulated, and measured. Each TPV in these structures has 55-μm via diameter, 366-μm via height, and 88° taper angle. The center-to-center pitch between signal (aggressor or victim) TPVs and adjacent ground TPVs is 150 μm, while the pitch between aggressor TPV and victim TPS is varied as 150 μm and 200 μm, resulting in different coupling strengths. To use the coplanar probe systems, the bottom sides of TPVs were left as open-circuit terminations, and the probes landed on the top side pads. The measured noise transfer functions are plotted in Figure 4.11, as well as those from the equivalent circuit model and 3D EM simulations. It is found that for both 150 μm and 200 μm coupling distances, the equivalent circuit model closely match the 3D EM simulations and the measurements. Therefore, the validity of the equivalent circuit model and the simulation setup has been verified through the measurements.

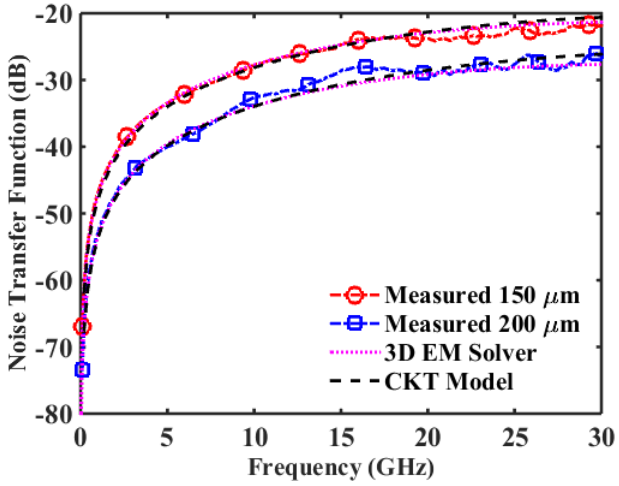


Figure 4.11: Measured noise transfer functions compared with the results from 3D EM solver and the equivalent circuit model.

To quantify the coupling from the equivalent circuit model, the inductive coupling coefficient (K_L) that is related to the inductive coupling from the magnetic fields, is

defined as the ratio of the mutual inductance to the self-inductance in (4.1)

$$K_L = \frac{L_m}{L_{\text{TPV}} + \frac{1}{2} \times L_{\text{TPV}}} \tag{4.1}$$

while the capacitive coupling coefficient (K_C) that is related to the capacitive coupling from the electric fields is defined as the ratio of the mutual capacitance to the total capacitance in (4.2)

$$K_C = \frac{C_m}{C_{GLS} + C_m}. \tag{4.2}$$

Then, 30-μm-diameter TPVs with various taper angles and various aspect ratios were simulated, and the inductive and capacitive coupling coefficients were computed from the simulations. Figure 4.12 (a) and (b) show that both inductive and capacitive coupling coefficients decrease with decreasing taper angles for various aspect ratios, indicating that tapered TPVs have less crosstalk. The reason is that via taper increases the self-inductance (L_{TPV}) but decreases the mutual capacitance (C_{m}), causing K_L and K_C to decrease. In addition, it is found from Figure 4.12 (c) and (d) that both inductive and capacitive coupling coefficients decrease with increasing aggressor-to-victim pitches for various aspect ratios, which can be attributed to the decreasing mutual inductance (L_{m}) and mutual capacitance (C_{m}). Hence, tapered TPVs have less inductive and capacitive couplings, and it is recommended to separate the victim TPV from the aggressor TPVs; the farther the better.

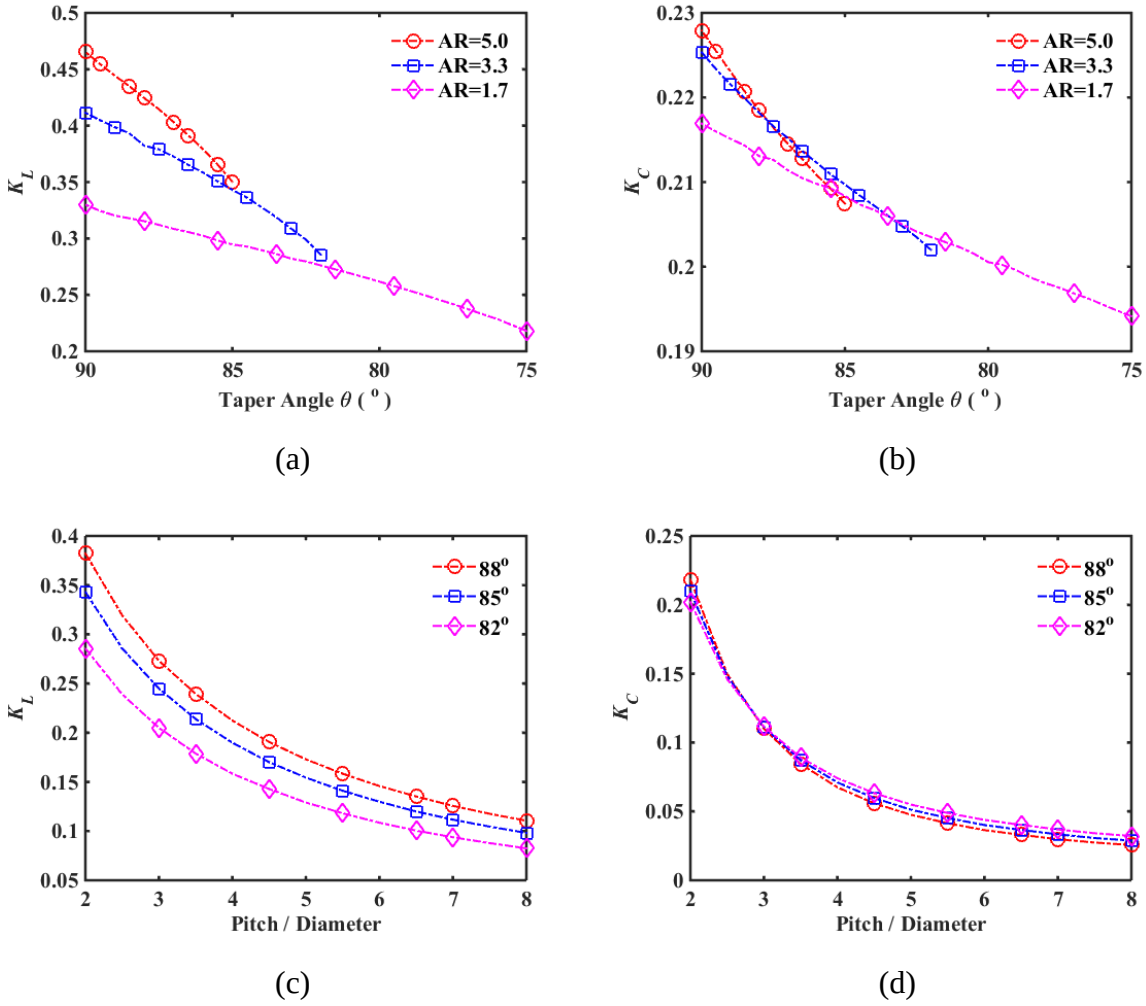
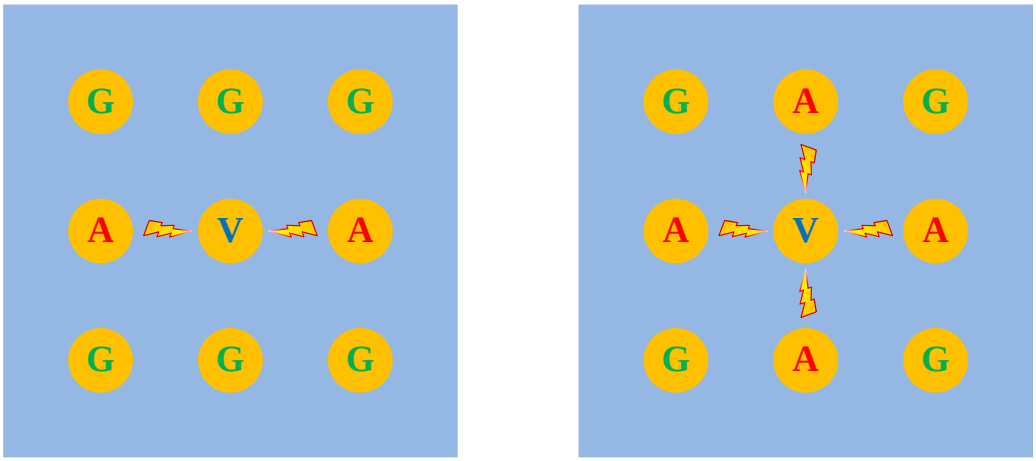


Figure 4.12: Simulated (a) inductive and (b) capacitive coupling coefficients vary with taper angles for 30-µm-diameter TPVs with 1.7/3.3/5.0 ARs; simulated (c) inductive and (d) capacitive coupling coefficients vary with aggressor-to-victim pitches for 30-µm-diameter TPVs with 88º/85º/82º taper angles.

4.3.2 Worst-Case Study

After studying the basic GSG-to-GSG coupling structure, two of the worst-case scenarios shown in Figure 4.13 were investigated. There are two aggressor TPVs adjacent to a victim TPV, as shown in Figure 4.13 (a), while four aggressor TPVs are adjacent to a victim TPV. Each TPV has 30-µm diameter, 100-µm height, and 88^o taper angle at

minimum 60-μm pitch between each other.



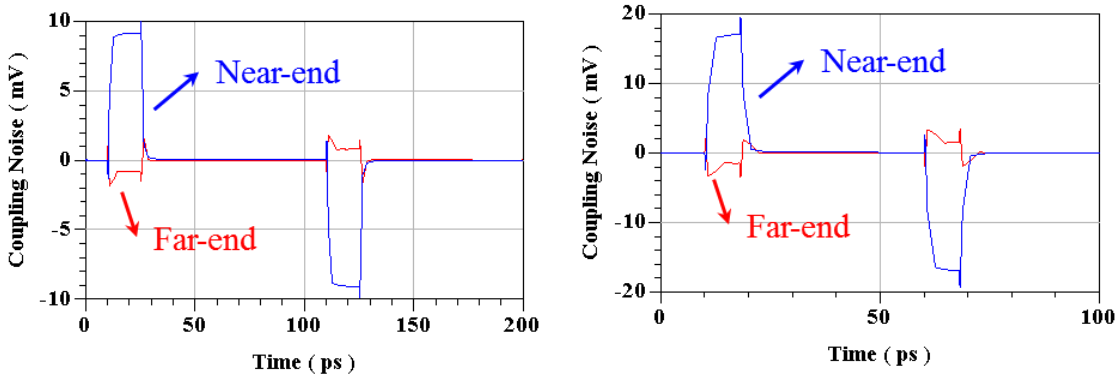
(a) (b)

Figure 4.13: Top view of two worst-case via configurations: (a) two aggressors and one victim (A2V1), and (b) four aggressors and one victim (A4V1).

Both scenarios were simulated using the 3D EM solver — HFSS in frequency domain, and then the *S*-parameters were imported into SPICE to perform the time-domain simulations. Similar to Figure 4.5, each aggressor TPV is connected to a voltage source on the top with 50 Ω impedance and time-periodic rectangular pulse trains that have 1 V high-level voltage and 0 V low-level voltage. The rise/fall time is 8 ps for 10 GHz pulse frequency and 15 ps for 20 GHz pulse frequency. While victim TPVs are terminated at each end with 50 Ω impedance, aggressor TPVs are terminated only at the bottom end.

The simulated near-end and far-end crosstalk noises of the victim TPV for two aggressors and one victim (A2V1) configuration are presented in Figure 4.14 (a) and (b) at the pulse frequency of 10 GHz and 20 GHz, respectively. The peak-to-peak voltages of the near-end crosstalk noises are 20 mV (2% or -33.98 dB) and 40 mV (4% or 27.96 dB), for 10 GHz and 20 GHz pulse frequencies, respectively, while the peak-to-peak voltages of the far-end crosstalk noises are 4 mV (0.4% or -47.96 dB) and 6 mV (0.6% or -44.44

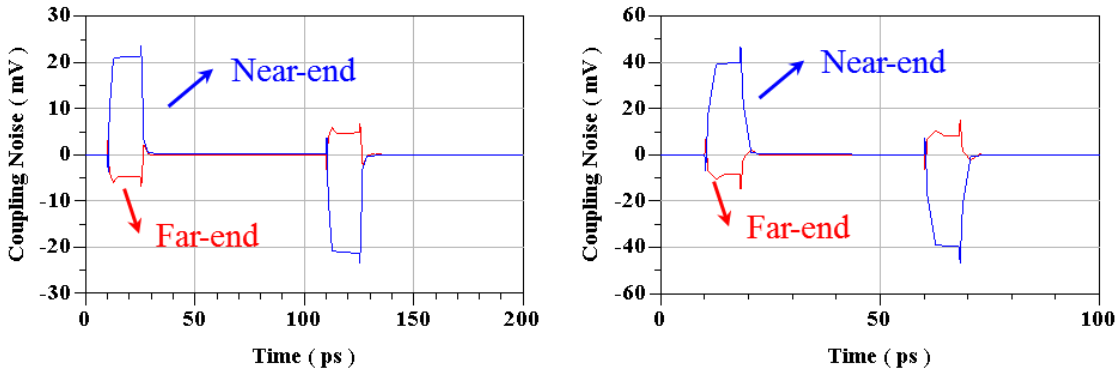
dB), for 10 GHz and 20 GHz pulse frequencies, respectively. Because the amplitude of the crosstalk noise is inversely proportional to the rise and fall time, reducing the pulse frequency to increase the rise and fall time is preferred for crosstalk reduction.



(a) (b)

Figure 4.14: Simulated near-end and far-end crosstalk noises of the victim TPV for two aggressors and one victim (A2V1) configuration at the pulse frequency of (a) 10 GHz and (b) 20 GHz.

Similarly, Figure 4.15 shows the simulated near-end and far-end crosstalk noises of the victim TPV for the four aggressors and one victim (A4V1) configuration at pulse frequencies of 10 GHz and 20 GHz. It is found that the peak-to-peak voltages of the near-end crosstalk noises are 48 mV (4.8% or -26.38 dB) and 94 mV (9.4% or -20.54 dB), for 10 GHz and 20 GHz pulse frequencies, respectively, while the peak-to-peak voltages of the far-end crosstalk noises are 14 mV (1.4% or -37.08 dB) and 30 mV (3% or -30.46 dB), for 10 GHz and 20 GHz pulse frequencies, respectively. By comparing Figure 4.14 and Figure 4.15, it can be concluded that doubling the number of aggressor TPVs to one victim TPV increases the crosstalk amplitude by more than twofold. Hence, when designing TPVs in glass interposers, it is preferred to keep the number of aggressor TPVs as low as possible.

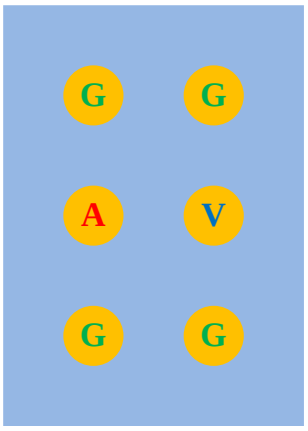


(a) (b)

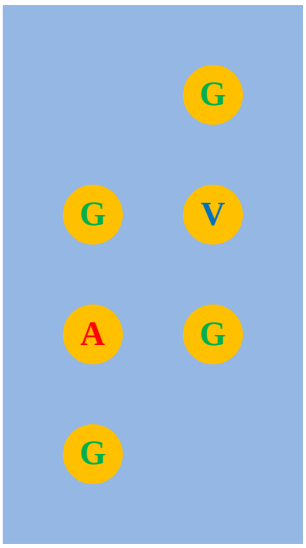
Figure 4.15: Simulated near-end and far-end crosstalk noises of the victim TPV for four aggressors and one victim (A2V1) configuration at the bit rate of (a) 10 Gbps and (b) 20 Gbps.

4.3.3 Suppression Techniques

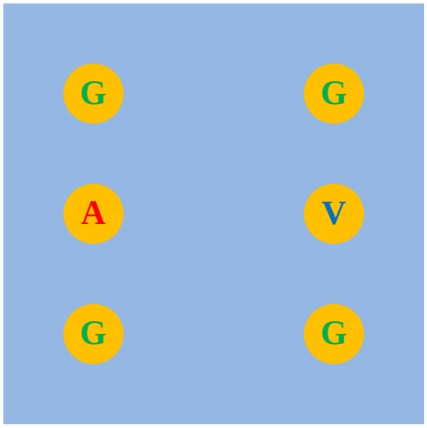
As described in Subsection 4.3.2, the noise coupling for some scenarios is larger than the target (-30 dB) for digital circuit applications. In addition, analog circuits, such as low-noise amplifiers, have stringent requirements for noise coupling. To suppress TPV coupling noises, five techniques are proposed and investigated, as shown in Figure 4.16. Figure 4.16 (a) shows the GSG-GSG configuration discussed in Sub-Section 4.3.1 as a reference for comparison; Figure 4.16 (b) shows the staggered GSG-GSG with aggressor and victim TPVs in a staggered pattern; Figure 4.16 (c) shows GSG-GSG with the aggressor-to-victim pitch increased by twofold; Figure 4.16 (d) shows GSG-GSG with a grounded via fence between aggressor and victim TPVs; Figure 4.16 (e) shows GSG-GSG in a rhombus-grounded Faraday cage; and Figure 4.16 (f) shows GSG-GSG in a full Faraday cage.



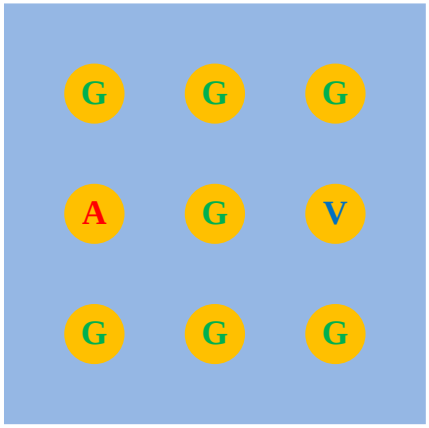
(a)



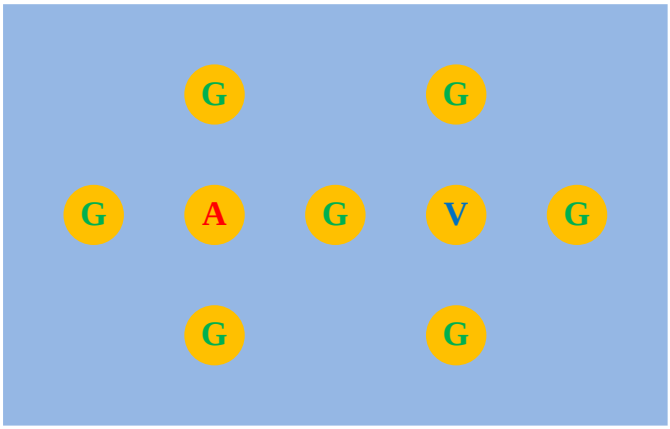
(b)



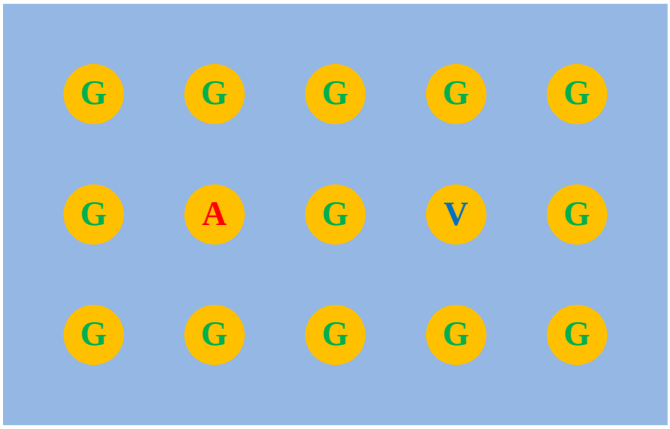
(c)



(d)



(e)



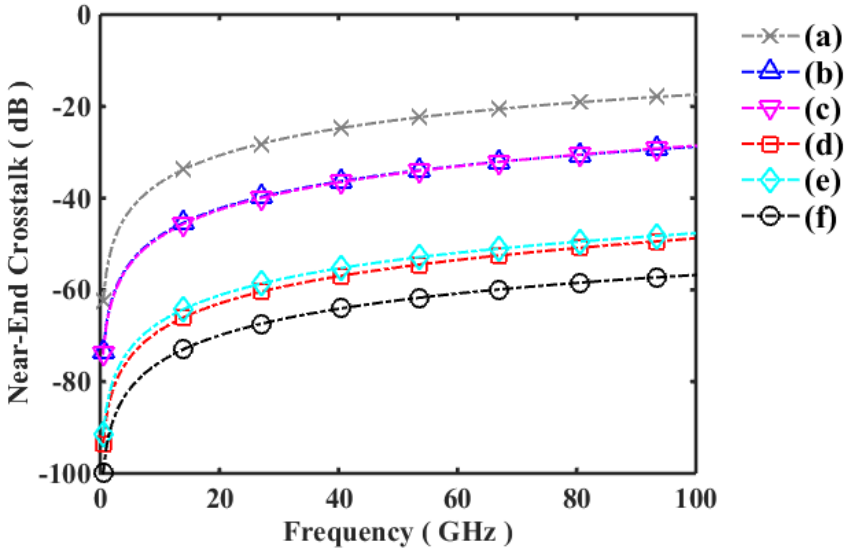
(f)

Figure 4.16: Top view of crosstalk suppression techniques: (a) GSG-GSG reference; (b) staggered GSG-GSG; (c) GSG-GSG with increased pitch; (d) GSG-GSG with a grounded via fence; (e) rhombus-grounded Faraday cage; (f) full Faraday cage.

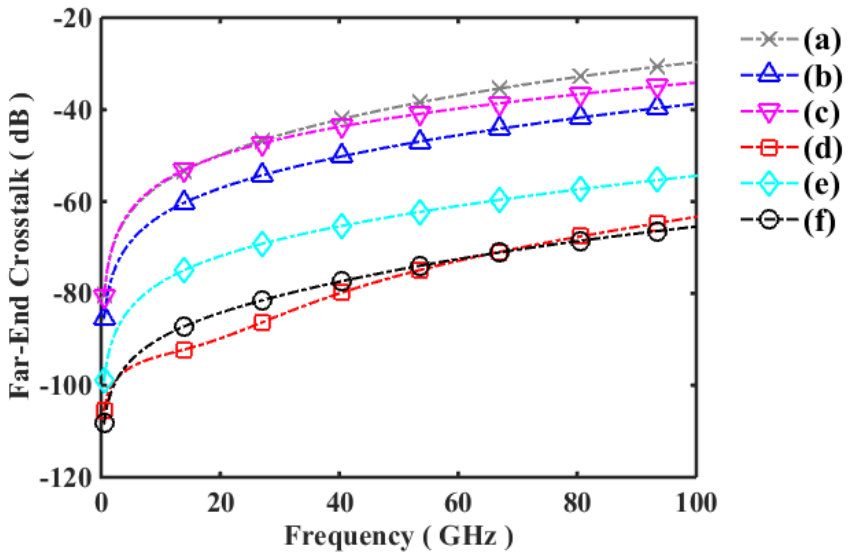
These via configurations were simulated using a 3D EM solver — HFSS, and the magnitudes of the near-end and far-end crosstalk for each via configuration are plotted in Figure 4.17 (a) and (b), respectively. The results are summarized in Table 4.1 for comparison. To achieve -30 dB isolation between aggressor and victim TPVs at frequencies up to 100 GHz, at least seven ground TPVs are required, and GSG-GSG with grounded via fence shown in Figure 4.16 (d) is preferred due to its compact size and minimum number of ground TPVs.

Table 4.1: Comparison between via configurations shown in Figure 4.16

	(a)	**(b)**	**(c)**	**(d)**	**(e)**	**(f)**
Near-end crosstalk (dB)	-17.4	-28.8	-28.6	-48.8	-47.7	-56.7
Far-end crosstalk (dB)	-29.7	-38.1	-34.1	-63.3	-54.4	-65.5
Footprint ($p \times p$)	1×2	1×3	2×2	2×2	4×2	4×2
No. of ground TPVs	4	4	4	7	7	13



(a)



(b)

Figure 4.17: Simulated magnitudes of (a) near-end crosstalk and (b) far-end crosstalk for GSG-GSG reference ( ), staggered GSG-GSG ( ), GSG-GSG with increased pitch ( ), GSG-GSG with grounded via fence ( ), rhombus-grounded Faraday cage ( ), and full Faraday cage ( ), as shown in Figure 4.16.

To quantitatively compare these via configurations, two figures of merit are defined as follows

$$\mathrm{FOM}_1 = \frac{\left|20\times\log_{10}\left(\sqrt{\mathrm{NEXT}\times\mathrm{FEXT}}\right)\right|}{\mathrm{area}} \tag{4.3}$$

$$\mathrm{FOM}_2 = \frac{\left|20\times\log_{10}\left(\sqrt{\mathrm{NEXT}\times\mathrm{FEXT}}\right)\right|}{\#_{\mathrm{GroundTPVs}}/\#_{\mathrm{SignalTPVs}}} \tag{4.4}$$

where NEXT and FEXT are the magnitudes of the near-end and far-end crosstalk, respectively, area is the footprint in unit of center-to-center pitch, and $\#_{\text{Ground TPVs}}$ and $\#_{\text{Signal TPVs}}$ are the numbers of ground and signal TPVs, respectively. As the near-end and far-end crosstalk are equally important, they are weighted equally in (4.3) and (4.4).

Based on the values listed in Table 4.1, two figures of merit were computed and summarized in Table 4.2 for comparison. In terms of crosstalk suppression per unit area, GSG-GSG with a grounded via fence shown in Figure 4.16 (d) is the only configuration that has a higher FOM_1 than GSG-GSG reference, which means that a larger footprint is required to achieve high crosstalk suppression. In terms of crosstalk suppression per unit number of ground TPVs, except for GSG-GSG in a full Faraday cage shown in Figure 4.16 (f), all of the other via configurations shown in Figure 4.16 (b)-(e) have higher FOM_2 than the GSG-GSG reference. As stated before, GSG-GSG with a grounded via fence shown in Figure 4.16 (d) is the preferred via configuration to achieve high crosstalk suppression.

It is important to mention that although the GSG-GSG in a rhombus-grounded Faraday cage shown in Figure 4.16 (e) is not as good as the GSG-GSG with a grounded via fence shown in Figure 4.16 (d), the GSG-GSG in a rhombus-grounded Faraday cage provides additional shielding on the leftmost and rightmost sides of the aggressor and victim TPVs, respectively. In addition, GSG-GSG in a full Faraday cage provides omnidirectional and best isolation between aggressor and victim TPVs. Therefore, while choosing one of the suppression techniques shown in Figure 4.16, design engineers have

to consider other factors, such as footprint and lateral shielding, in addition to the isolation requirement.

Table 4.2: Comparison of figures of merit between via configurations

	(a)	**(b)**	**(c)**	**(d)**	**(e)**	**(f)**
FOM_1	11.78	11.15	7.84	14.01	6.38	7.64
FOM_2	11.78	16.73	15.68	16.01	14.59	9.40

4.4 Summary

In this chapter, the design of tapered TPVs in glass interposer for improved signal integrity was presented, covering the aspects of signal transition, impedance discontinuity, and crosstalk.

The effect of via taper on the signal transition was first studied in frequency and time domains through *S*-parameters and eye diagrams, respectively. The results show that the via taper has negative impacts on the *S*-parameters, and as the aspect ratio increases, these effects are exacerbated, but even for the TPVs with worst taper angle (75^o) at 100 GHz, the S_{21} magnitude is still greater than -1 dB (90%). In addition, the eye-diagram analysis shows that unlike the noticeable degeneration of the eye diagrams for the case of TSVs in silicon interposers, TPVs in glass interposers are almost electrically transparent. Even though the taper improves the eye diagrams of TSVs in silicon interposers, it does not have significant impact for TPVs in glass interposers.

The impedance discontinuity of TPVs in glass was analyzed through time-domain reflectometry (TDR), which was found to be inductive. The results show that as the taper angle decreases and the aspect ratio increases, the maximum impedance in the TDR response increases, exceeding the 5% design tolerance. Thus, two effective via

configurations, namely GSG and four ground TPVs with a signal TPV (G4S1), were proposed to minimize this impedance discontinuity.

Lastly, the GSG-to-GSG TPV crosstalk structure was investigated. An equivalent circuit model was developed for analysis, and it was verified against 3D EM simulations and measurements in the frequency domain. Based on the equivalent circuit model, it was found that both inductive and capacitive coupling coefficients decrease with decreasing taper angles and increasing aggressor-to-victim pitches. Two of the worst-case scenarios were studied. The results conclude that reducing the pulse frequency to increase the rise and fall time and keeping the number of aggressor TPVs as low as possible are preferred for crosstalk reduction. In addition, five effective design techniques were proposed and investigated to suppress crosstalk noise. By comparing these techniques, it was concluded that while GSG-GSG in a full Faraday cage provides the highest omnidirectional isolation between aggressor and victim TPVs, it requires a large footprint and multiple ground TPVs. GSG-GSG with grounded via fence is the preferred choice, as it achieves more than 30 dB isolation with compact size and minimum number of ground TPVs.

CHAPTER 5

MILLIMETER-WAVE CHARACTERIZATION OF TAPERED TPVS

In this chapter, the electrical parasitics associated with TPVs in glass are experimentally characterized up to 50 GHz using two different methods, namely a short-circuit method and a ring-resonator method. Each method models a single TPV as a resistor in series with an inductor, because the inductance is the most dominant factor for TPVs in glass, as discussed in CHAPTER 3, and the parasitic resistance and inductance of TPVs can impact the PDN impedance and change the impedance profile of decoupling capacitors. Accurate measurement of the via resistance and inductance are important to reduce design iteration cycles, and are also critical for channel budgeting.

The short-circuit method is a one-port structure with a TPV shorting the signal to the backside ground plane, generating a reflection to the incident signal. The ring-resonator method involves inserting TPVs in the middle of a capacitively coupled ring structure, thus altering the original resonant modes. An equivalent circuit including via parasitics and a transmission-line based equivalent network were proposed for short-circuit and ring-resonator methods, respectively. In addition, the sensitivity of each method with respect to via resistance and inductance was studied. Based on the two methods, test vehicles were designed and fabricated using a panel-scalable double-sided metallization process. The test structures were measured using a vector network analyzer (VNA) with ground-signal-ground (GSG) probes. Finally, the resistance and inductance of a single via were extracted from the measured *S*-parameters, for both the short-circuit method and the ring-resonator method, and these methods were compared in terms of footprint and accuracy.

5.1 Short-Circuit Method

The short-circuit method utilizes a one-port structure with all GSG TPVs connected to the backside ground plane. By measuring the reflected signal, the via parasitics can be retrieved. An equivalent circuit was proposed for this method to relate the input impedance of TPVs to the *S*-parameters, and the sensitivity of the *S*-parameters with respect to via resistance and inductance was derived.

5.1.1 Equivalent Circuit Analysis

The short-circuit method was initially proposed in [55, 56] to characterize the series resistance and inductance of TSVs. The structure based on this methodology is shown in Figure 5.1, with a signal TPV shorting the signal to the backside ground. The backside ground is constructed to be a solid plane rather than a trace, in that a ground plane has negligible inductance for perfect shorting. In addition, the probing pad is based on the coplanar waveguide (CPW) for 50 Ω impedance match, and the pad length is minimized to reduce the pad inductance.

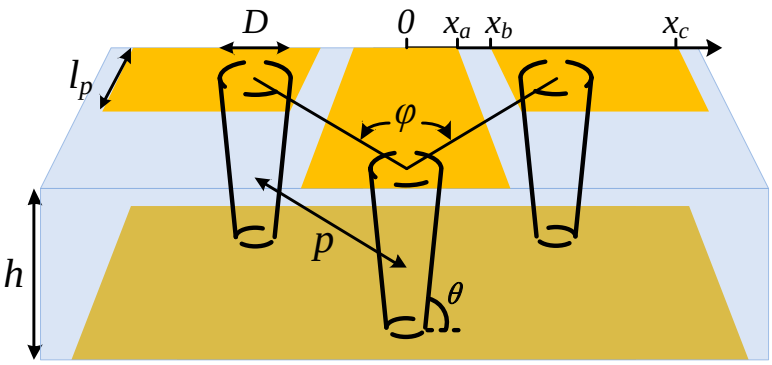


Figure 5.1: Perspective view of the short-circuit structure with TPVs shorted at the backside for retrieving resistance and inductance.

Based on the geometric structure of Figure 5.1, an equivalent circuit model was proposed, as shown in Figure 5.2. There are a total of three TPVs in this scenario, namely

two return or ground TPVs and one signal TPV, where each TPV is modelled as a resistor (R_{TPV}) in series with an inductor (L_{TPV}). The parasitic capacitance and conductance between signal and return TPVs, respectively denoted by C_{GLS} and G_{GLS}, can be computed based on the concept presented in CHAPTER 3 with the expressions in [69]. For the Ground–Signal–Ground (GSG) probe, one signal pad and two ground pads are directly on these TPVs, and the parasitic pad capacitance denoted by C_{pad} exist between them, which can be computed by the expressions in [70]. Due to the symmetry of the GSG configuration, the current flowing through each of the two return TPVs is estimated to be half of that in the signal TPV.

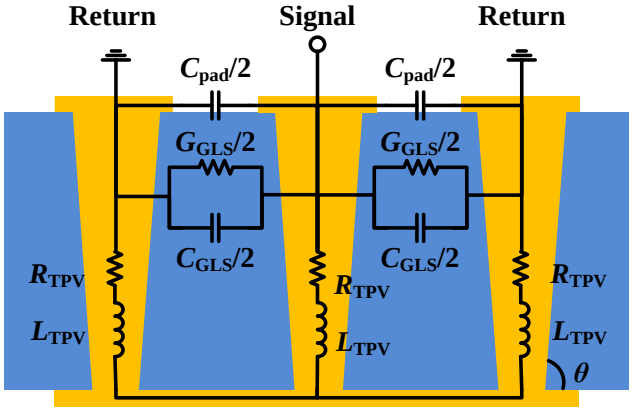


Figure 5.2: Equivalent circuit model of the short-circuit structure.

Therefore, the input impedance of the short-circuit structure can be derived from the equivalent circuit model as

$$Z_{in} = \frac{1}{j\omega\left(C_{pad} + C_{GLS}\right) + G_{GLS}} + \frac{3}{2}\left(R_{TPV} + j\omega L_{TPV}\right) \tag{5.1}$$

where C_{pad} is the parasitic pad capacitance, C_{GLS} and G_{GLS} are the parasitic capacitance and conductance of glass, respectively, R_{TPV} and L_{TPV} are the resistance and inductance of each TPV, respectively, and $\omega = 2\pi f$ is the radian frequency.

Probing on the short-circuit structure by GSG on-wafer probes, its *S*-Parameters can be measured using a vector network analyzer (VNA), which are then converted into

Z-parameters. Since this structure is a one-port network, the obtained *S*-parameter is essentially the reflection coefficient (S_{11} or Γ), which is related to the *Z*-parameters by the following equation [62]

$$Z_{\text{in}} = Z_{\text{s}} \times \frac{1+S_{11}}{1-S_{11}} \tag{5.2}$$

where Z_s is the reference impedance, typically 50 Ω. As the via impedance is relatively small, especially at low frequency, S_{11} is close to 1, resulting in a small value in the denominator in (5.2). Therefore, the noise from the measurement (ΔS_{11}) will be magnified in (5.2) and propagate to the measured resistance and inductance. Hence, the short-circuit method requires a high-precision measurement to accurately characterize TPVs.

5.1.2 Sensitivity Analysis

The parasitic resistance and inductance of TPVs are related to the reflection coefficient – S_{11} – through Z_{in}. To understand this relation between the parasitics of TPVs and the reflection coefficient, the sensitivity of S_{11} magnitude with respect to the resistance and inductance is derived from

$$S_{11} = \frac{Z_{\text{in}} - Z_{\text{s}}}{Z_{\text{in}} + Z_{\text{s}}}. \tag{5.3}$$

First, the sensitivity of S_{11} with respect to Z_{in} is expressed as

$$\frac{\partial S_{11}}{\partial Z_{\text{in}}} = \frac{2Z_{\text{s}}}{\left(Z_{\text{in}} + Z_{\text{s}}\right)^2}. \tag{5.4}$$

As Z_{in} is the input impedance of the short-circuit structure, it is related to the parasitic resistance and inductance through (5.1), and its partial derivative to the via resistance and inductance can be expressed as

$$\frac{\partial Z_{\text{in}}}{\partial R_{\text{TPV}}} = \frac{3}{2} \tag{5.5}$$

$$\frac{\partial Z_{\text{in}}}{\partial L_{\text{TPV}}} = \frac{3}{2} \cdot j\omega . \tag{5.6}$$

Hence, the sensitivity of S_{11} magnitude with respect to the resistance and inductance is

$$\frac{\partial |S_{11}|}{\partial R_{\text{TPV}}} = \left| \frac{\partial S_{11}}{\partial Z_{\text{in}}} \cdot \frac{\partial Z_{\text{in}}}{\partial R_{\text{TPV}}} \right| \tag{5.7}$$

$$\frac{\partial |S_{11}|}{\partial L_{\text{TPV}}} = \left| \frac{\partial S_{11}}{\partial Z_{\text{in}}} \cdot \frac{\partial Z_{\text{in}}}{\partial L_{\text{TPV}}} \right| . \tag{5.8}$$

Substituting (5.4) and (5.5) into (5.7), the sensitivity of S_{11} magnitude with respect to resistance is computed up to 50 GHz, and the results are depicted in Figure 5.3. It is found that the sensitivity of S_{11} magnitude increases with increasing frequency, while the resistance variation does not have a significant impact on the sensitivity. In addition, the value of the sensitivity shown in the color scale of Figure 5.3 indicates that the S_{11} magnitude is slightly sensitive to the resistance, making the short-circuit method challenging for resistance characterization.

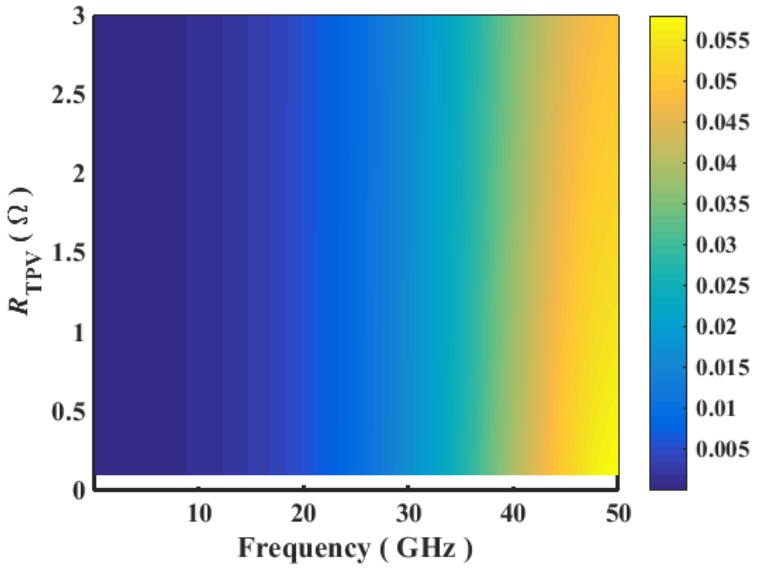


Figure 5.3: Sensitivity of $|S_{11}|$ with respect to various via resistances across 0.1-50 GHz.

Similarly, by substituting (5.4) and (5.6) into (5.8), the sensitivity of S_{11} magnitude with respect to inductance is computed and the results are shown in Figure 5.4. For a given inductance value, the sensitivity of S_{11} magnitude peaks at a certain frequency that decreases as the inductance increases, but below and beyond this frequency, the sensitivity decreases. In addition, the value of the color scale shows that the sensitivity with respect to inductance is much more significant than that to resistance because of the *jw* term in (5.6), suggesting that the experimental characterization of the via inductance is easier than the characterization of the via resistance.

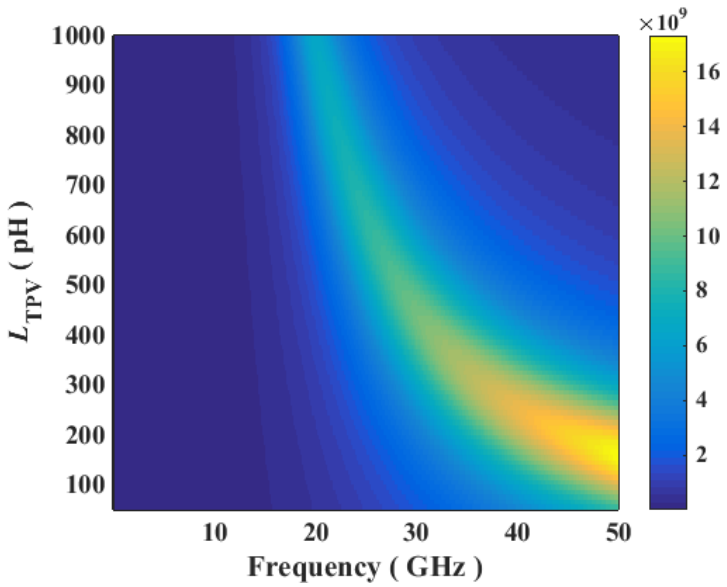


Figure 5.4: Sensitivity of $|S_{11}|$ with respect to various via inductances across 0.1-50 GHz.

5.2 Ring-Resonator Method

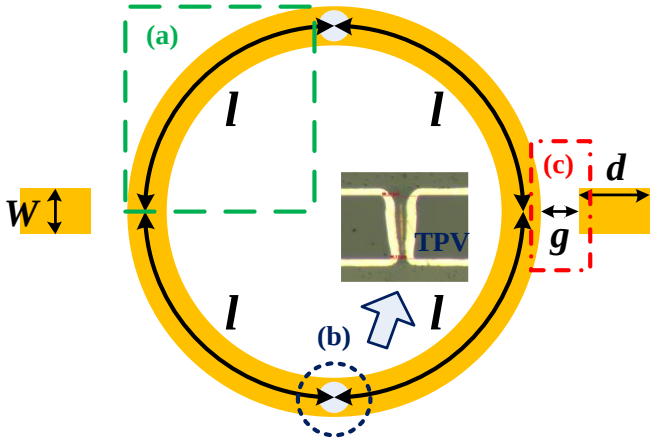
To improve the sensitivity of the short-circuit method, especially with respect to via resistance, a ring-resonator method is proposed in this section. An original ring resonator is a capacitively coupled ring structure, and the ring-resonator method is to insert TPVs in the middle. By doing so, the original resonant modes will be selectively altered, and the via parasitics will induce additional resonances due to the extra length of

TPVs. Thus, at the TPV-induced resonances, via parasitics can be retrieved from the *S*-parameters. An equivalent network based on the transmission-line model was proposed for fundamental analysis of this method, and the sensitivity of this method was studied with respect to via resistance and inductance.

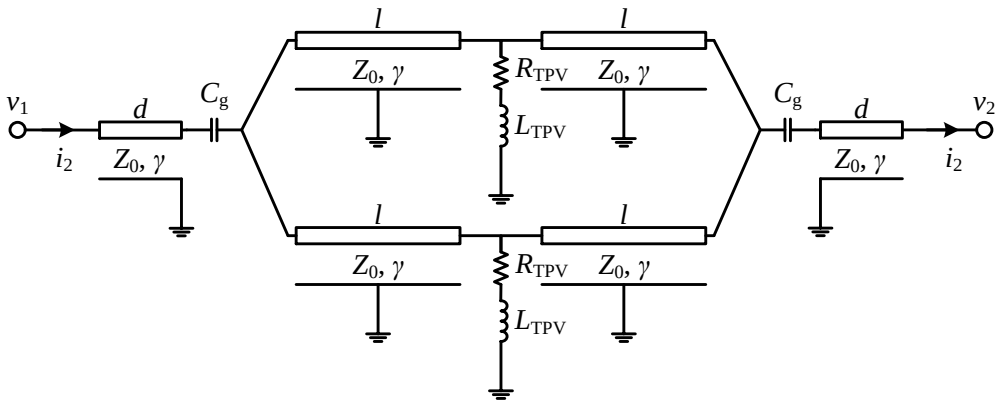
5.2.1 Equivalent Network Analysis

Equivalent Network

The ring resonator is one of the most commonly used methods for characterizing the substrate permittivity and the loss tangent. In the case of a microstrip-based ring resonator, if TPVs are inserted in the middle of the ring - shorting the signal line to the bottom ground plane - the original resonant modes will be altered. The microstrip-based ring resonator structure with TPVs is illustrated in Figure 5.5 (a), and the corresponding equivalent network based on the transmission-line model is proposed in Figure 5.5 (b). The mean circumference of the ring is $4\times l$, while the microstrip feed is separated from the ring by a distance *g*. Both the ring and the micostrip feed have a trace width of *W*.



(a)



(b)

Figure 5.5: (a) Top view of the ring resonator structure with TPVs in the middle, and (b) its equivalent network.

The proposed equivalent network can be decomposed into three basic elements: (a) quarter of the ring, (b) the TPV in the middle of the ring, and (c) the capacitive coupling gap between the microstrip feed and the ring. The quarter of the microstrip ring is modeled as transmission lines, while each TPV is modeled as a resistor in series with an inductor because the inductance dominates in glass substrate. Previously-reported research works model the coupling gap as a π-network or an L-network. However, when the gap is small enough, the series capacitance C_g will dominate and by itself is sufficient to model this gap discontinuity.

ABCD Matrix Analysis

The *ABCD* matrix is used to analyze the equivalent network shown in Figure 5.5 (b). The *ABCD* matrix of the upper or lower half of the whole ring with TPVs in the middle is computed by cascading the transmission line model for one quarter of the ring, the equivalent circuit for the TPV, and the transmission line model for the second quarter of the ring as below:

$$\begin{bmatrix} A_{R/2} & B_{R/2} \\ C_{R/2} & D_{R/2} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ Y_0 \sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ Y_v & 1 \end{bmatrix} \times \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ Y_0 \sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \tag{5.9}$$

where γ is the propagation constant which can be extracted from the simulation of the microstrip line in a 2D EM solver, l is one quarter of the mean ring circumference, $Z_0 = 1/Y_0$ is the characteristic impedance of the microstrip ring resonator, and Y_v is the input admittance of each TPV. The only unknown parameter needed to retrieve the input admittance Y_v is the propagation constant γ, while l and Z_0 are design parameters. Based on (5.9), the *ABCD* matrix of the whole ring in Figure 5.5 (a) can be presented as

$$\begin{bmatrix} A_R & B_R \\ C_R & D_R \end{bmatrix} = \begin{bmatrix} A_{R/2} & B_{R/2}/2 \\ 2 \cdot C_{R/2} & D_{R/2} \end{bmatrix} = \begin{bmatrix} \cosh(2\gamma l) + Z_0 Y_v \dfrac{\sinh(2\gamma l)}{2} & \dfrac{Z_0^2 Y_v \sinh^2(\gamma l) + Z_0 \sinh(2\gamma l)}{2} \\ 2Y_v \cosh^2(\gamma l) + 2Y_0 \sinh(2\gamma l) & \cosh(2\gamma l) + Z_0 Y_v \dfrac{\sinh(2\gamma l)}{2} \end{bmatrix}. \tag{5.10}$$

After cascading with the coupling capacitance C_g of the capacitive coupling gap computed by the formulae in [71], the *ABCD* matrix of the entire structure can be expressed as

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A_R + Z_C \cdot C_R & B_R + Z_C(A_R + D_R) + Z_C^2 \cdot C_R \\ C_R & D_R + Z_C \cdot C_R \end{bmatrix} \tag{5.11}$$

where A_R, B_R, C_R and D_R are the matrix elements in (5.10), and Z_C is the impedance of the serious capacitance C_g, which is calculated as

$$Z_C = 1/j\omega C_g . \tag{5.12}$$

Finally, the *ABCD* matrix in (5.11) is converted to *S*-parameters, and the admittance Y_v of each TPV is related to the S_{21} by the following equation

$$Y_v \cdot \mathrm{X}_1 + \mathrm{X}_2 = \frac{2}{S_{21}} \tag{5.13}$$

with

$$Y_v = \left(R_{\mathrm{TPV}} + j\omega L_{\mathrm{TPV}}\right)^{-1} \tag{5.14}$$

$$\mathrm{X}_1 = Z_0 \sinh(2\gamma l)\cdot\left(1+\frac{Z_C}{Z_\mathrm{s}}\right)+\frac{Z_0^2 \sinh^2(\gamma l)}{2Z_\mathrm{s}}+2\cosh^2(\gamma l)\cdot\left(\frac{Z_C^2}{Z_\mathrm{s}}+2Z_C+Z_\mathrm{s}\right) \tag{5.15}$$

$$\mathrm{X}_2 = 2\cosh(2\gamma l)\cdot\left(1+\frac{Z_c}{Z_\mathrm{s}}\right)+\frac{Z_0 \sinh(2\gamma l)}{2Z_\mathrm{s}}+2Y_0 \sinh(2\gamma l)\cdot\left(\frac{Z_C^2}{Z_\mathrm{s}}+2Z_C+Z_\mathrm{s}\right) \tag{5.16}$$

where Z_s is the reference impedance, typically 50 Ω, and S_{21} is the *S*-parameter from the left capacitive coupling gap to the right capacitive coupling gap.

5.2.2 Resonance and Sensitivity Analysis

In this section, we explain the fact that inserting TPVs alters the resonant modes of the original ring resonator using S_{21}. In addition, the sensitivity of the S_{21} magnitude with respect to via resistance and inductance is numerically derived and analyzed.

TPV-Induced Resonance

Figure 5.6 presents the calculated S_{21} magnitude for the 9 GHz ring resonators with and without TPVs in the middle. The resonant frequencies of the ring resonator without TPVs are divided into odd-order and even-order frequencies.

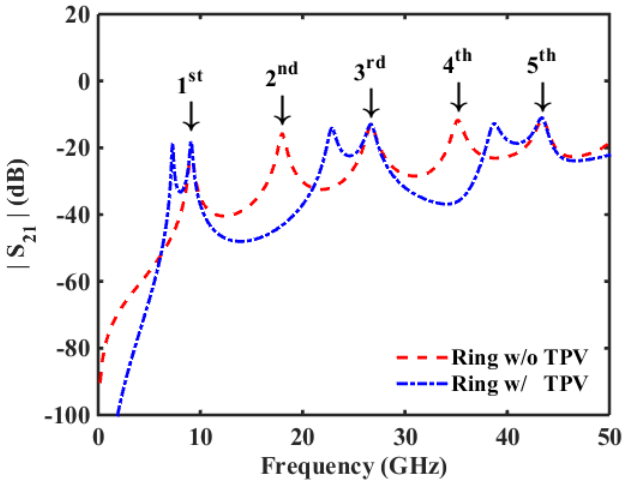


Figure 5.6: Comparison of calculated S_{21} magnitude for 9 GHz ring resonator with and without TPVs in the middle.

At the odd-order frequencies, one quarter of the mean ring circumference (*l*), can be expressed as

$$l = \lambda/4 + n \cdot \lambda/2 \ (n = 0, 1, 2, \cdots). \tag{5.17}$$

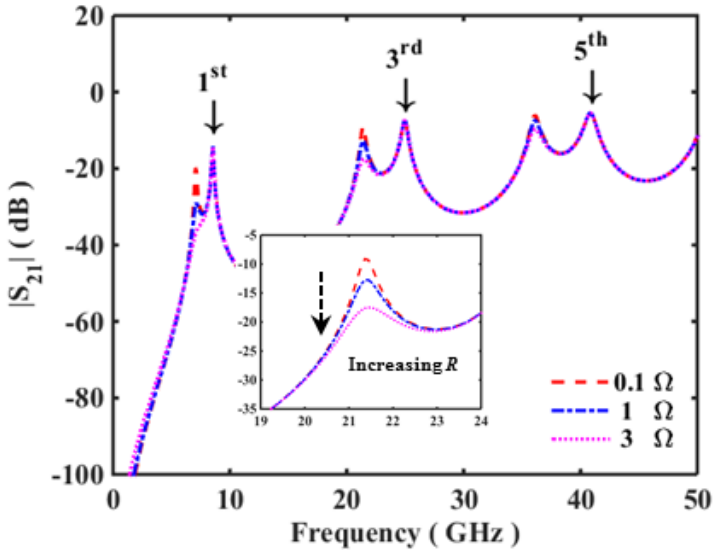
Inserting TPVs in the middle of the ring will not affect these resonant modes, since the capacitive coupling gap can be treated as an open circuit [72], and the length *l* forms a quarter-wave transformer — transforming the open circuit to the short circuit in the middle of the ring. Thus, at these odd-order frequencies, the middle of the ring acts as the short circuit or perfect electrical conductor (PEC) boundary condition, and inserting TPVs will not alter these resonant modes. More importantly, due to the extra length of these TPVs, another resonance will be introduced slightly below each odd-order resonant frequency, as shown in Figure 5.6. On the other hand, at the even-order frequencies, *l* is expressed as

$$l = m \cdot \lambda/2 \ (m = 0, 1, 2, \cdots). \tag{5.18}$$

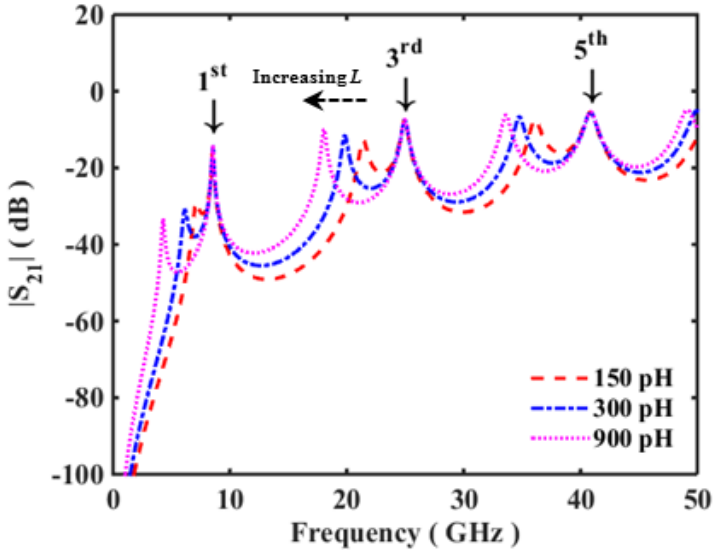
The middle of the ring behaves as the open circuit by the half-wave transformer, but the inserted TPVs will physically short the signal to the ground, which violates the condition

for the even-order resonant modes. Therefore, at these even-order frequencies, the inserted TPVs in the middle of the ring will eliminate these resonances.

In addition, the S_{21} magnitude for various parasitic resistances and inductances was computed by the proposed equivalent network, and the results are presented in Figure 5.7. As shown in Figure 5.7 (a), increasing via resistance dampens S_{21} magnitude at the resonances induced by the TPVs in the middle of the ring. Also, as shown in Figure 5.7 (b), increasing TPV inductance lowers the TPV-introduced resonant frequency. Detailed sensitivity of S_{21} magnitude with respect to via resistance and inductance will be presented shortly.



(a)



(b)

Figure 5.7: Simulated S_{21} magnitude by the proposed equivalent network for (a) various resistances and (b) various inductances.

Sensitivity Study

As shown in Figure 5.7 , increasing resistance will lower the S_{21} magnitude at the resonances, while increasing inductance will lower the resonant frequencies. In this sub-section, the sensitivity of S_{21} magnitude with respect to resistance and inductance is derived using (5.13). First, the sensitivity of S_{21} with respect to Y_v is expressed as

$$\frac{\partial S_{21}}{\partial Y_v} = \frac{-2X_1}{(X_1 \cdot Y_v + X_2)^2}. \tag{5.19}$$

Since Y_v is the input admittance of the TPV, its partial derivative to via resistance and inductance can then be calculated as

$$\frac{\partial Y_v}{\partial R_{TPV}} = -(R_{TPV} + j\omega L_{TPV})^{-2} \tag{5.20}$$

$$\frac{\partial Y_v}{\partial L_{TPV}} = -j\omega \cdot (R_{TPV} + j\omega L_{TPV})^{-2}. \tag{5.21}$$

Thus, the sensitivity of S_{21} magnitude with respect to resistance and inductance is

$$\frac{\partial|S_{21}|}{\partial R_{TPV}} = \left|\frac{\partial S_{21}}{\partial Y_v} \cdot \frac{\partial Y_v}{\partial R_{TPV}}\right| \tag{5.22}$$

$$\frac{\partial|S_{21}|}{\partial L_{TPV}} = \left|\frac{\partial S_{21}}{\partial Y_v} \cdot \frac{\partial Y_v}{\partial L_{TPV}}\right|. \tag{5.23}$$

Substituting (5.19) and (5.20) into (5.22), the sensitivity of S_{21} magnitude with respect to resistance is computed up to 50 GHz for a 9 GHz ring resonator with TPVs in the middle, and the results are depicted in Figure 5.8. It is found that the S_{21} magnitude is only sensitive to TPV resistance at the TPV-induced resonant frequencies, namely 7.0 GHz, 21.4 GHz, and 36.2 GHz, and varying resistance will not alter the resonant frequencies. Furthermore, at each resonant frequency, the sensitivity decreases with the resistance increase, which implies that the ring-resonator method is appropriate for TPV characterization as via resistance is typically small.

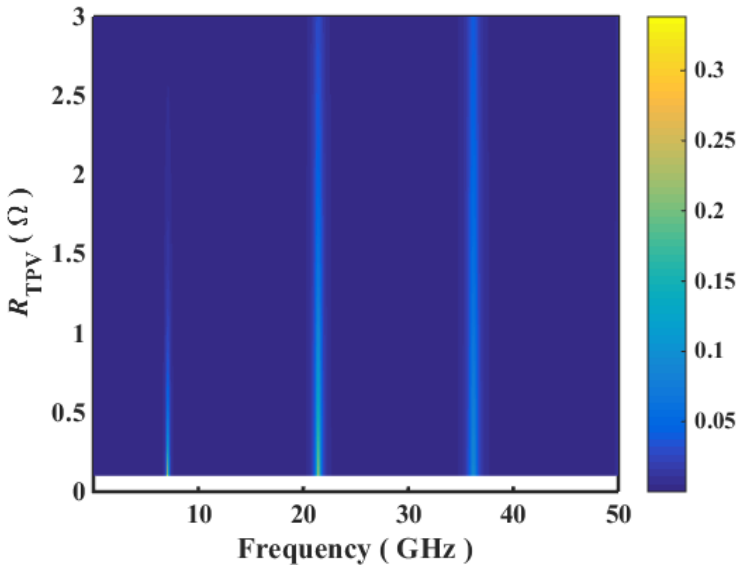


Figure 5.8: Sensitivity of S_{21} magnitude with respect to various TPV resistances across 0.1-50 GHz.

Similarly, by substituting (5.19) and (5.21) into (5.23), the sensitivity of S_{21} magnitude with respect to inductance is computed and the results are shown in Figure 5.9. The sensitivity of S_{21} magnitude also decreases with the increase in via inductance. However, varying inductance will change the resonant frequencies, in contrast to the frequency-independent behavior with respect to resistance. As the inductance increases, the resonant frequencies decrease rapidly to begin with and then eventually saturate. In addition, the sensitivity with respect to inductance is more significant than that to resistance because of the $j\omega$ term in (5.21).

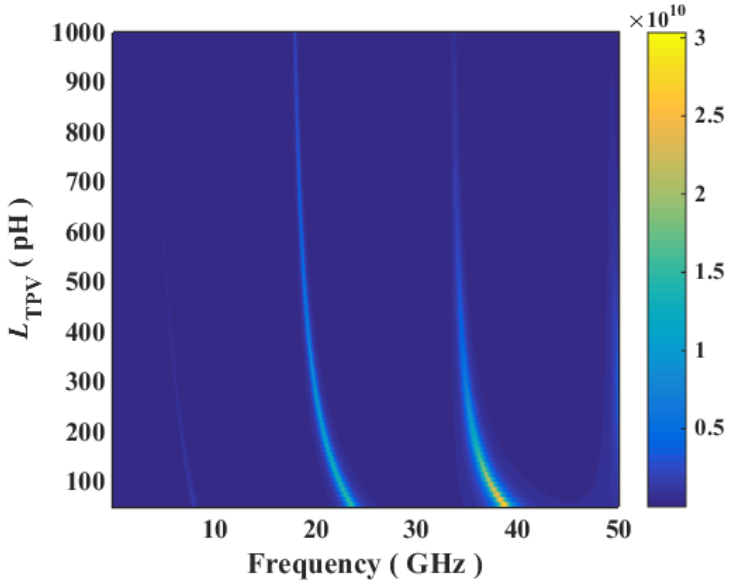


Figure 5.9: Sensitivity of S_{21} magnitude with respect to various TPV inductances across 0.1-50 GHz.

5.3 Test Vehicle Design and Fabrication

Based on the aforementioned short-circuit and ring-resonator methods, test vehicles were designed on Asahi Glass Company (AGC) EN-A1 glass with high-aspect-ratio TPVs. Two short-circuit coupons with circular and square via pads were designed, and three ring resonators were designed at 3 GHz, 6 GHz, and 9 GHz as fundamental

frequencies. The test vehicle was also fabricated using a novel process targeting low-cost panel-based manufacturability.

5.3.1 Test Vehicle Design

Short-Circuit Design

The perspective view of the short-circuit design is illustrated in Figure 5.10, and the design parameters are summarized in Table 5.1. The CPW probing pad is designed to match an impedance of 50 Ω and also to accommodate GSG probes at 250-μm pitch. The pad length is slightly greater than the minimum length required for the probe landing, and thus the pad-introduced inductance is minimized. The thickness of the glass substrate was 300 μm for better handling during fabrication, and TPVs were formed by the focused electrical-discharge method developed by AGC, with 55-μm via diameter and 175-μm center-to-center via pitch.

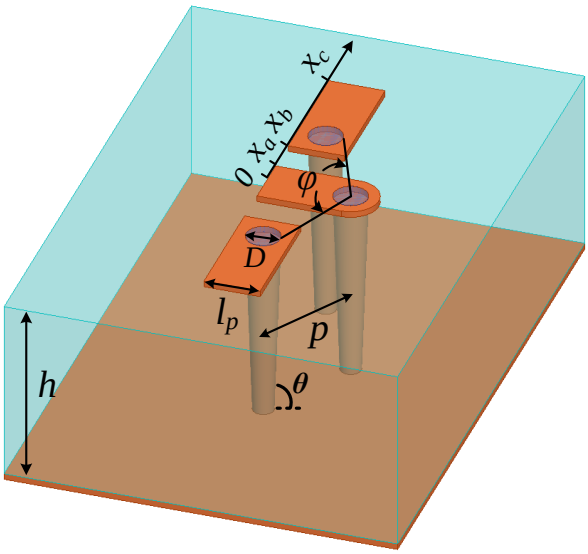


Figure 5.10: Perspective view of the short-circuit design.

Table 5.1: Summary of design parameters for short-circuit method

Symbol	Quantity	Value
x_a	CPW signal conductor position	45 μm
x_b	CPW gap position	105 μm
x_c	CPW ground conductor position	300 μm
l_p	CPW pad length	90 μm
D	TPV diameter	55 μm
θ	TPV taper angle	88°
p	Signal-to-return TPV pitch	175 μm
φ	Angle between signal and two return TPVs	118°
h	Substrate thickness	366 μm

Ring-Resonator Design

The perspective view of the ring-resonator design is illustrated in Figure 5.11, and the design parameters are summarized in Table 5.2. The CPW probing pad is the same as the one on the short-circuit design, as well as the glass substrate and TPVs. The microstrip line was designed for a 50 Ω characteristic impedance, and three ring resonators were designed for the fundamental frequencies at 3 GHz, 6 GHz, and 9 GHz, to cover a wide frequency range. The capacitive gap is a tradeoff between the coupling strength and the minimum feature size in fabrication. The microstrip feed line was purposely tapered to connect the 50 Ω CPW probing pad to the 50 Ω microstrip line with minimum reflection.

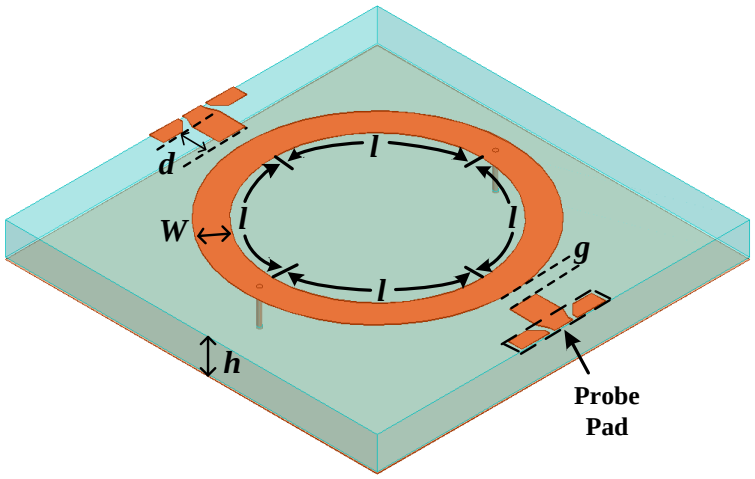


Figure 5.11: Perspective view of the ring-resonator design.

Table 5.2: Summary of design parameters for ring-resonator method

Symbol	Quantity	Value
D	TPV diameter	55 µm
h	Substrate thickness	366 µm
θ	TPV taper angle	88°
W	Microstrip line width	680 µm
l	1/4 of the ring circumference	4.441 mm 6.667 mm 13.344 mm
g	Capacitive gap width	40 µm
d	Microstrip feed line length	150 µm

5.3.2 Fabrication Process

As mentioned in CHAPTER 2, glass substrate with high-aspect-ratio TPVs can be metallized using the advanced CMOS process. However, this process is not a low-cost solution, and its scalability is not good for large-volume manufacturing of glass

interposers. Thus, a panel-scalable double-sided process for metallizing high-aspect-ratio TPVs in glass substrates is developed and depicted in Figure 5.12. The TPVs in bare glass were first formed by a focused electrical-discharge method, with the entry via diameter of 55 μm, via height of 300 μm, and a taper angle of 88 deg. Next, a low-viscosity polymer was laminated on each side of the glass, and then, the polymer in the TPVs was removed by UV laser ablation. Finally, a semi-additive process (SAP), one of the most common processes for the substrate fabrication, was used to metallize such high-aspect-ratio TPVs.

The complete fabrication process starts with 300-μm glass substrate prepared by the glass supplier, and the TPVs in glass are formed by its via-drilling method, which is referred to as focused electrical-discharge method. Then, the glass substrate is laminated with a 33-μm polymer on each side, introduced to enhance the adhesion of the copper to the smooth glass surface and also to prevent glass from cracking. Since the TPVs in glass are completely filled with polymer after lamination, as shown in Figure 5.13 (a), a UV laser ablation is used to open the TPVs. Subsequently, the electro-less plating is used to deposit a 0.4-μm copper seed layer over the surface of the polymer-laminated glass substrate. After the seed-layer deposition, the substrate is patterned on both sides using lithography. Following this, an electrolytic copper plating is used to increase the copper thickness to 10 μm as illustrated in Figure 5.13 (b). Then the photoresist is stripped, and the copper seed layer is micro-etched away, completing the fabrication process.

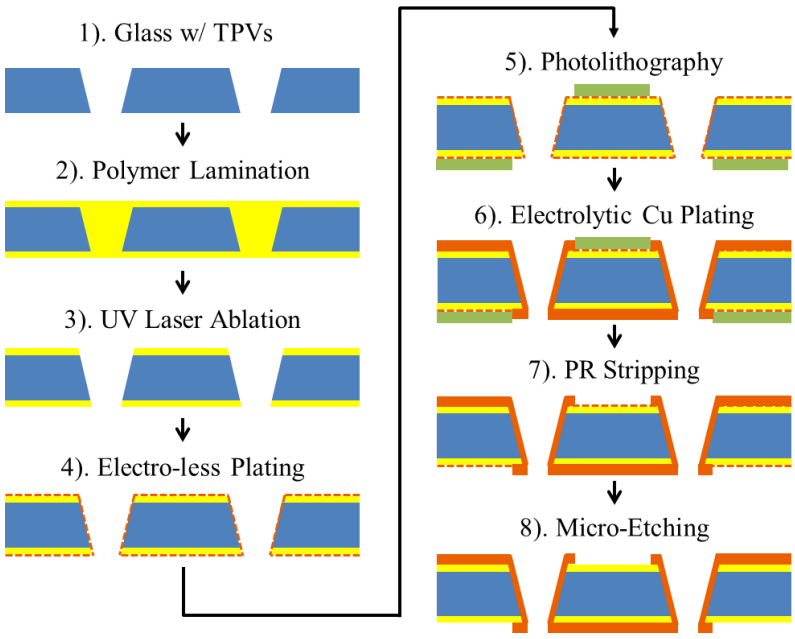
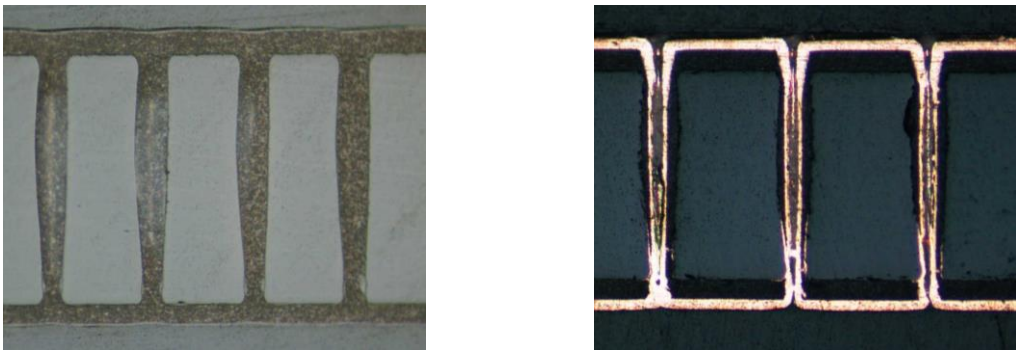


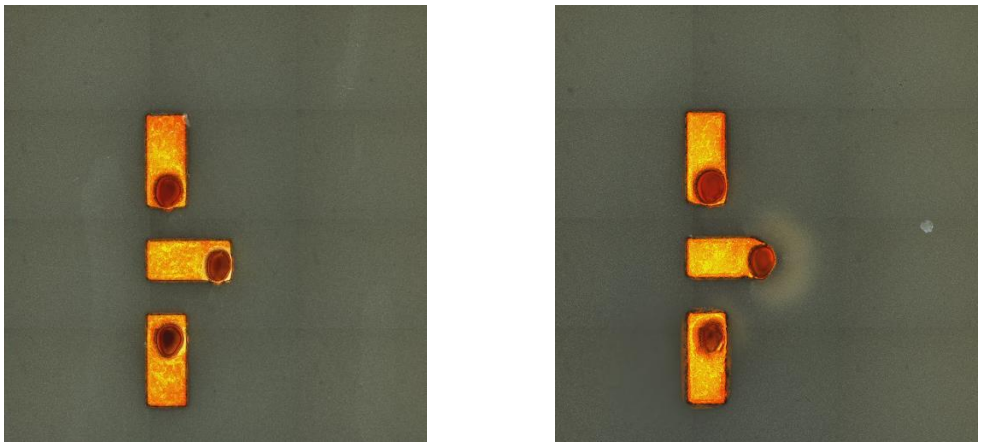
Figure 5.12: Process flow for metallizing high-aspect-ratio TPVs in glass.



(a) (b)

Figure 5.13: Cross-section view of the TPVs in glass (a) after polymer lamination, and (b) after electrolytic Cu plating.

The top view of two fabricated short-circuit coupons is presented in Figure 5.14, and the top view of the fabricated 9 GHz ring resonator with TPVs in the middle is presented in Figure 5.15. The test vehicles were also measured up to 50 GHz, and the measured results, as well as more detailed interpretation of the data, will be presented in Section 5.4.



(a) (b)

Figure 5.14: Top view of two fabricated short-circuit coupons.

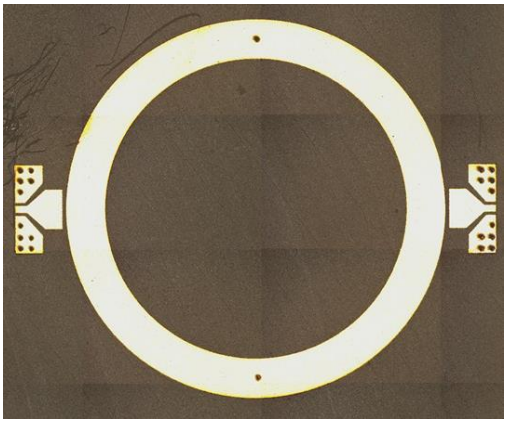


Figure 5.15: Top view of the fabricated 9 GHz ring resonator with TPVs in the middle.

5.4 Results and Discussion

After the fabrication of the test vehicle, substrate-probing measurements were performed from 0.01 MHz to 50 GHz using the Agilent VNA E8361C and the Cascade Microtech GSG probes. Then, the via resistance and inductance were retrieved from the measured *S*-parameters based on the principles of the short-circuit method and the ring-

resonator method presented in Section 5.1 and 5.2, respectively. Finally, these methods are compared in terms of accuracy and footprint.

5.4.1 Measurement Results

The two-port Short-Open-Load-Through (SOLT) calibration was used to correct the systematic errors of the entire measurement system including VNA, coaxial cables, and GSG probes. As the short-circuit designs are one-port structures, one GSG probe was landed for measurement, while two GSG probes were landed for the two-port ring-resonator designs

Short-Circuit Method

In an ideal case, TPVs should have no resistance or inductance. From the perspective of the impedance Smith Chart shown in Figure 5.16, the ideal TPV is supposed to be located in the leftmost point of the impedance Smith Chart. Unfortunately, there is series resistance with each TPV because of the finite copper conductivity. Also, due to the skin effect, the input impedance moves from the outermost circle into the inside of the impedance Smith Chart. More importantly, the inductance introduced by the physical length of the TPV plays a critical role for high-speed digital applications, which might cause overshooting or simultaneous switching noise. This inductance effect makes the input impedance travel along the outermost circle. Thus, the skin effect and the inductance effect of the TPV result in the impedance moving along the impedance Smith Chart to the inside.

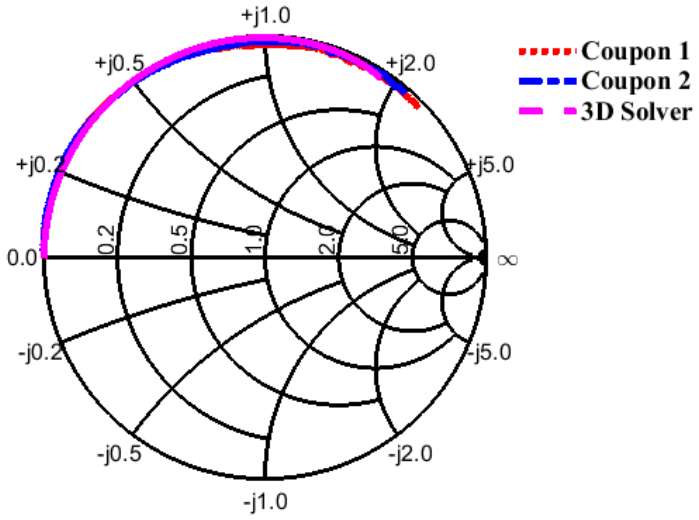


Figure 5.16: Measured and simulated *S*-parameters shown in the Impedance Smith Chart.

Once the *S*-parameters were obtained, they were converted into *Z*-parameters by (5.2). Then, according to (5.1), the resistance and the inductance of each TPV can be calculated as,

$$R_{\mathrm{TPV}} = \frac{2}{3}\cdot \mathrm{Re}\left\{ Z_{\mathrm{s}} \times \frac{1+S_{11}}{1-S_{11}} - \frac{1}{j\omega\left(C_{\mathrm{pad}}+C_{\mathrm{GLS}}\right)+G_{\mathrm{GLS}}} \right\} \tag{5.24}$$

$$L_{\mathrm{TPV}} = \frac{2}{3\cdot\omega}\cdot \mathrm{Im}\left\{ Z_{\mathrm{s}} \times \frac{1+S_{11}}{1-S_{11}} - \frac{1}{j\omega\left(C_{\mathrm{pad}}+C_{\mathrm{GLS}}\right)+G_{\mathrm{GLS}}} \right\} \tag{5.25}$$

where S_{11} is the measured reflection coefficient, C_{GLS} and G_{GLS} can be computed by the idea presented in CHAPTER 3 with the expressions in [69], C_{pad} can computed by the expressions in [70].

In Figure 5.17, it can be seen that the resistance of a single TPV is small and very challenging to measure. At 10 GHz, the simulated resistance was around 100 mΩ, which is close to the measured resistances with an average value of around 185 mΩ. Due to the skin effect, the resistance increases as frequency increases. In addition, the measured

resistance has noise as expected, because the sensitivity of the short-circuit method with respect to resistance is relatively low, as discussed in Sub-Section 5.2.2.

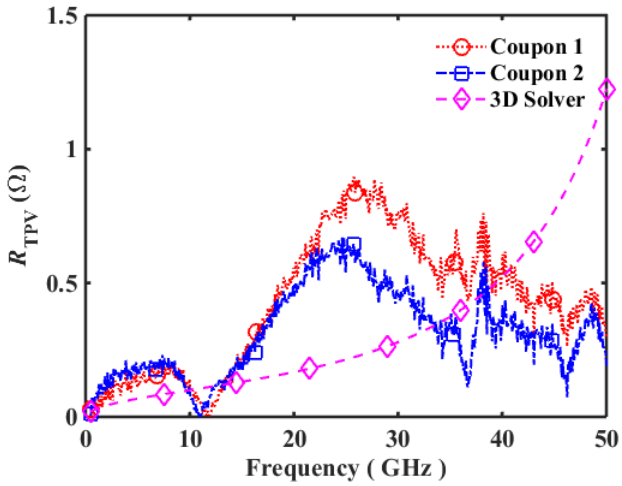


Figure 5.17: Resistance retrieved from the measured and simulated *S*-parameters.

The extracted inductance is plotted in Figure 5.18, and the measured results match well with the simulated ones. The inductance of a single via was estimated to be 140 pH at 10 GHz which is much lower than the typical values for wire-bond interconnects, generally in the nH order of magnitude. The inductance decreases with frequency, because the skin effect causes the TPV to lose its internal inductance.

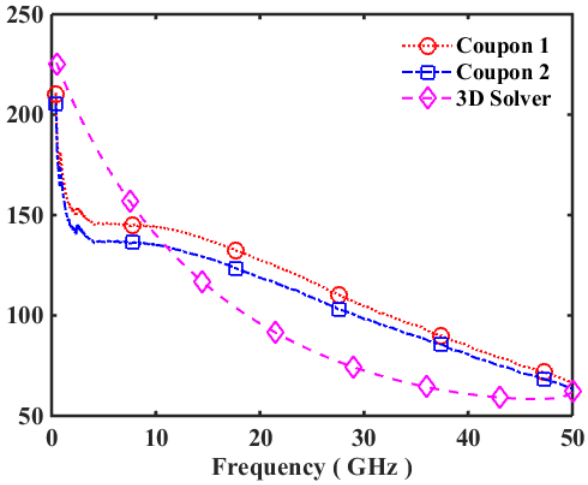


Figure 5.18: Inductance retrieved from the measured and simulated *S*-parameters.

A minor mismatch is seen below 2 GHz between the measured inductance and the simulated inductance. The reason is that the inductance effect is not as pronounced at these low frequencies, and the sensitivity of this method with respect to inductance is lower at low frequencies than that at high frequencies, which makes the measurement challenging. In addition to these, the proximity effect also increases the mismatch between modeling and measurement, especially at high frequency. The magnitude of the magnetic field at 20 GHz around the TPV is shown in Figure 5.19. According to the boundary condition of the magnetic field below

$$\vec{J}_S = \hat{n} \times \vec{H} \tag{5.26}$$

the current flowing in the signal via is almost uniformly distributed along the via circumference. However, it is not the case for the two return vias, as shown in Figure 5.19. The magnetic field is almost crowded in half of the return via while the other half is not contributing much to the current conduction. In other words, the assumption in Figure 5.2, that the return via is electrically identical to signal via, is good but not very precise, considering the proximity effect.

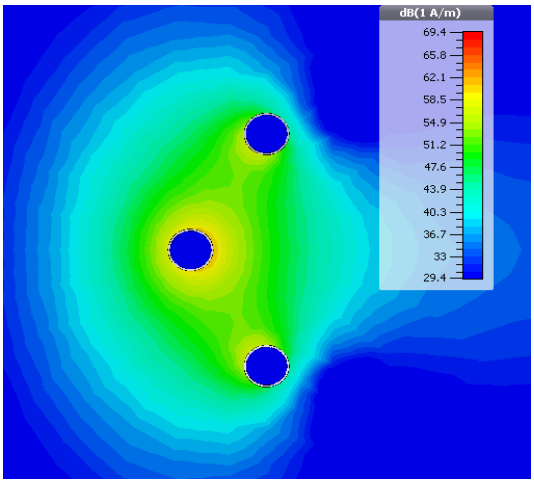
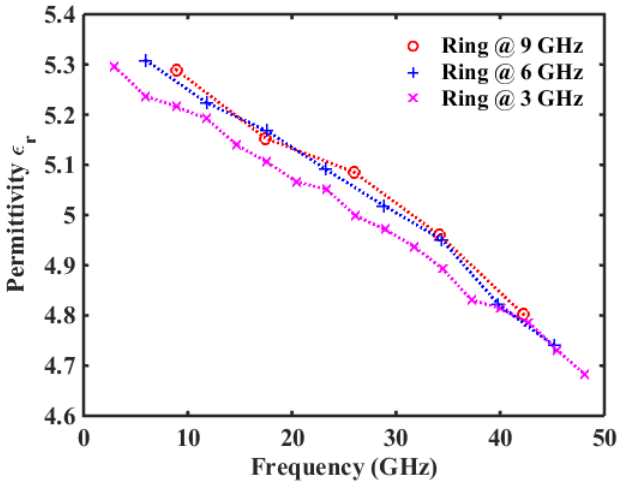


Figure 5.19: Magnitude of the magnetic field at 20 GHz surrounding the TPV array.

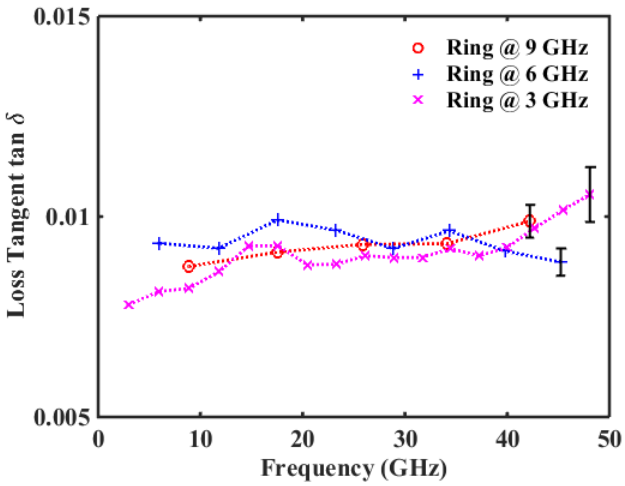
Ring-Resonator Method

(a) Substrate Characterization

As mentioned in Sub-Section 5.3.1, the propagation constant γ used in (5.15) and (5.15) is the only unknown parameter, and it is critical for retrieving via resistance and inductance. Since it highly depends on the electrical properties of the substrate, the ring resonators without TPVs in the middle were measured to extract the dielectric constant and the loss tangent of the polymer-laminated glass substrate up to 50 GHz, as shown in Figure 5.20. The dielectric constant and the loss tangent extracted from 3 GHz, 6 GHz, and 9 GHz ring resonators are identical to each other, where the dielectric constant is decreasing with frequencies while the loss tangent is nearly constant over the frequency range. At 29 GHz, the dielectric constant and the loss tangent of this inhomogeneous substrate are averaged to be 5.0 and 0.0092, respectively, and was used in 3D EM solver – HFSS [67] to obtain the propagation constant γ. The declining trend of the dielectric constant with frequency results from the manufacturing process of adding sodium carbonate, calcium oxide, magnesium oxide and aluminum oxide in silica to lower the glass transition temperature and the CTE.



(a)



(b)

Figure 5.20: (a) Extracted dielectric constant and (b) extracted loss tangent of 366-µm polymer-laminated glass using 3 GHz, 6 GHz, and 9 GHz ring resonators.

(b) TPV Characterization

Based on the extracted dielectric constant and loss tangent, the resistance and inductance can be retrieved using the ring-resonator method and (5.13)-(5.16). The retrieved resistance is plotted in Figure 5.21, while the retrieved inductance is plotted in Figure 5.22. It can be seen from Figure 5.21 that the measured resistances from the three ring resonators are closely matched and they increase with increase in frequency because of the skin effect. The values of the resistance retrieved from three ring resonators are summarized in Table 5.3. As seen in Figure 5.22, the via inductance retrieved by the ring resonator method deceases with the increase in frequency. This is because with the increase in frequency, the current tends to flow in the TPV surface, reducing internal inductance. The specific values of the TPV inductance retrieved from the three ring resonators are given in Table 5.4. The close match of the via resistance and inductance between measurement and 3D EM simulation confirms the repeatability of the measurement and the feasibility of the ring-resonator method.

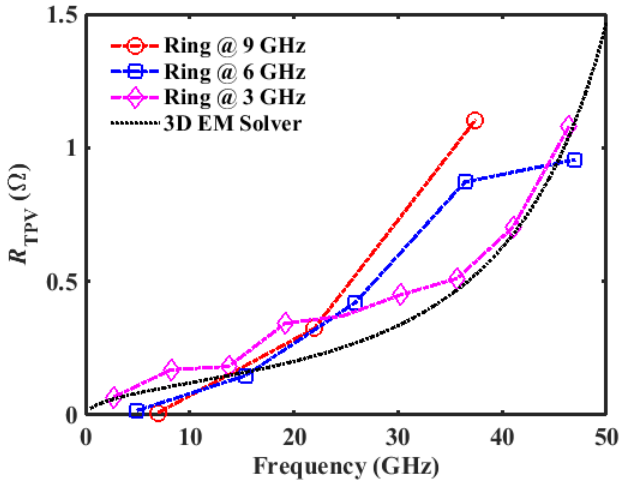


Figure 5.21: TPV resistance retrieved from the measured S_{21} using the ring-resonator method.

Table 5.3: Retrieved resistance from the ring resonator method

Ring	Symbol	Value								
3 GHz	f (GHz)	2.7	8.2	13.7	19.2	24.7	30.2	35.7	41.0	46.4
	R_{TPV} (Ω)	0.067	0.169	0.182	0.344	0.371	0.450	0.511	0.703	1.079
6 GHz	f (GHz)	5.0		15.3		25.9		36.5		47.0
	R_{TPV} (Ω)	0.047		0.147		0.421		0.873		0.955
9 GHz	f (GHz)	7.0			21.9			37.4		
	R_{TPV} (Ω)	0.083			0.324			1.105		

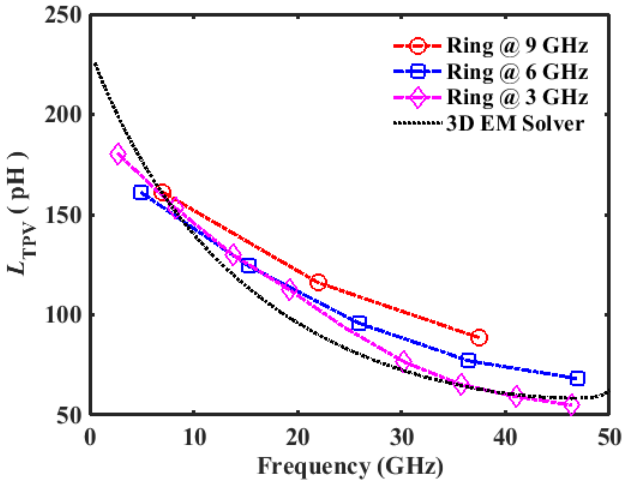


Figure 5.22: TPV inductance retrieved from the measured S_{21} using the ring-resonator method.

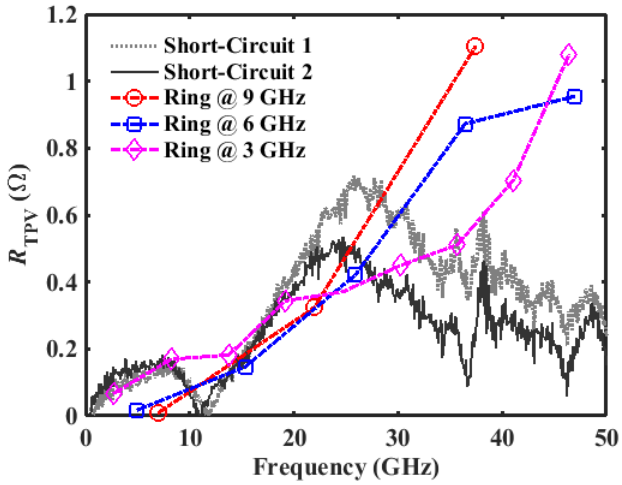
Table 5.4: Retrieved inductance from the ring resonator method

Ring	Symbol	Value								
3 GHz	f (GHz)	2.7	8.2	13.7	19.2	24.7	30.2	35.7	41.0	46.4
	L_{TPV} (pH)	180.5	153.4	130.0	112.5	93.0	76.5	65.2	59.1	54.9
6 GHz	f (GHz)	5.0		15.3		25.9		36.5		47.0
	L_{TPV} (pH)	161.0		124.3		95.9		77.1		68.1
9 GHz	f (GHz)	7.0			21.9			37.4		
	L_{TPV} (pH)	161.3			116.1			88.6		

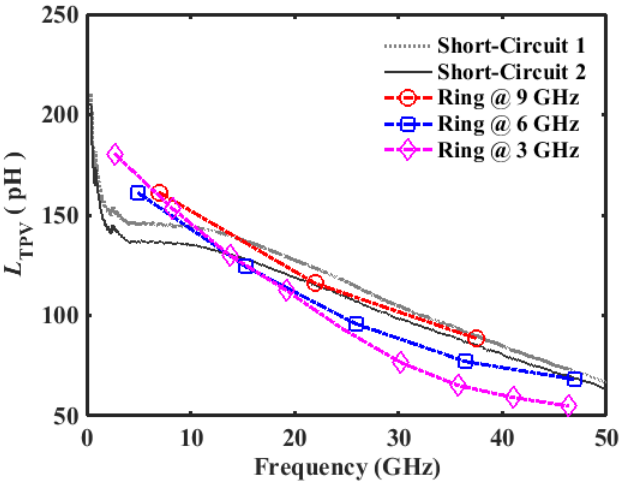
5.4.2 Method Comparison

The measured TPV resistance and inductance from the short-circuit method and the ring-resonator method are plotted in Figure 5.23 for comparison. Figure 5.23 (a) shows that the measured TPV resistance values from each method do not match well. Based on the sensitivity analyses presented in Sub-Section 5.1.2 and 5.2.2, it can be inferred that the short-circuit method is less sensitive to via resistance than the ring-

resonator method. However, it can be seen from Figure 5.23 (b) that the measured TPV inductance values from two methods are closely matched. The reason is that both the short-circuit method and the ring-resonator method have strong sensitivity with respect to via inductance. As shown in Table 5.5, the accuracy of the ring-resonator method is boosted by 1.60 times over the short-circuit method for resistance characterization, while the accuracy is increased by about 1.03 times for inductance characterization. Therefore, the ring-resonator method can characterize via resistance more accurately than the short-circuit method, and both methods can characterize via inductance accurately.



(a)



(b)

Figure 5.23: Comparison between the short-circuit method and the ring-resonator method in terms of the retrieved (a) TPV resistance and (b) TPV inductance.

In addition, the footprint for each method is compared in Table 5.5. The short-circuit design is compact, with dimensions 1.44×1.26 mm^2. However, the ring-resonator deign needs a large footprint to accommodate the ring structure. The smallest design is the 9 GHz ring resonator, with dimensions 8.01×8.42 mm^2 which is about 37 times larger than the short-circuit design.

In conclusion, the short-circuit method is not accurate for TPV resistance characterization, but it utilizes compact geometric structure; the ring-resonator method occupies large footprint, but it has high precision for TPV characterization.

Table 5.5: Comparison between short-circuit method and ring-resonator method

		Short-Circuit Method	**Ring-Resonator Method**
Accuracy	R_{TPV}	$\geq 39.8\%$	$\geq 63.6\%$
	L_{TPV}	$\geq 80.5\%$	$\geq 83.3\%$
Footprint		$\approx 1.44 \times 1.26$ mm^2	$\geq 8.01 \times 8.42$ mm^2

5.5 Summary

This chapter demonstrates two methods, namely the short-circuit method and the ring-resonator method, for experimentally characterizing TPVs in glass up to millimeter-wave frequencies. The short-circuit method is a one-port structure, with a TPV shorting the signal to the backside ground, generating a reflection to the incident signal, and the ring-resonator method is a two-port structure, with TPVs inserted in the middle of an original ring resonator to short the signal to the ground.

An equivalent circuit was used for the short-circuit method to relate the *S*-parameters to the input impedance of TPVs, while an equivalent network based on the transmission-line model was used to analyze the ring-resonator method. Furthermore, the sensitivity of each method with respect to resistance and inductance was investigated. The results show that the short-circuit method is much less sensitive to via resistance than via inductance, and the ring-resonator method is only sensitive to via resistance and inductance at specific resonant frequencies.

Based on the two methods, glass substrate test vehicles were designed and fabricated by a novel low-cost panel-compatible process with high-aspect-ratio TPVs. Two short-circuit coupons, as well as three ring resonators at 3 GHz, 6 GHz, and 9 GHz, were measured up to 50 GHz using VNA and on-wafer probes. Then, the TPV resistance and inductance were extracted from the measured *S*-parameters, and the measured values closely match those from 3D EM solver. For a 55-μm TPV in a 366-μm-thick glass substrate, the measured resistance and inductance are ~1 Ω and 60 pH at 40 GHz, respectively.

Finally, these two methods were compared in terms of accuracy and footprint. Compared to the short-circuit method, the accuracy achieved by the ring-resonator method is improved by about 1.60 times for via resistance and 1.03 times for via inductance. However, the footprint of the short-circuit method is 37 times smaller than that of the ring-resonator method.

CHAPTER 6

RESEARCH SUMMARY, CONCLUSIONS AND FUTURE WORK

This dissertation presented one of the first systematic and comprehensive studies on the electrical modeling, design, and characterization of tapered through-package vias (TPVs) in glass interposers for power delivery and signal transition.

To achieve highest data bandwidth per unit of power at lowest cost, 3D glass interposers with ICs on both sides of the interposer interconnected by fine pitch TPVs were proposed and demonstrated as a superior alternative to 3D IC stacking and 2.5D silicon interposers. However, TPVs in glass have a taper shape, and the taper angle varies from 75° to 88°, depending on the TPV formation methods. The objectives of this research were to model, design, and characterize the electrical performance of tapered TPVs in glass interposers to provide design guidelines for TPVs by quantifying their impact on electrical performance. Although there have been a number of such studies on the design of through-silicon vias (TSVs) in silicon, design guidelines for TPVs in glass for high performance applications has not been well documented.

The following fundamental challenges were identified to achieve the thesis goals: 1) the accuracy and the computational efficiency for precise via modeling; 2) the impedance discontinuity and the crosstalk induced by TPVs; 3) the accurate wideband measurement of TPVs with redistribution layers (RDLs) de-embedding. To address the aforementioned challenges, three research tasks were carried out: 1) electrical modeling of TPVs by taking into account both geometric and material effects; 2) design of TPVs for minimum impedance discontinuity and crosstalk; 3) millimeter-wave characterization of TPVs to extract via parasitics.

The data and analyses presented in the previous chapters proves that the research objectives were met successfully. This chapter summarizes the research outcomes of this

dissertation with key scientific and technical contributions and potential future work. A list of the published papers and awards is also provided.

6.1 Research Summary

6.1.1 Electrical Modeling of Tapered TPVs

1) Circuit Model: A wideband scalable circuit model was proposed to model tapered TPVs in glass, with analytical or semi-analytical equations derived for the *RLCG* parameters. The convergence study showed that as long as the tapered TPVs were sliced by more than 10 pieces, the convergence error was less than 10%. The *S*-parameters computed from the proposed model were compared with those from the 3D EM solver, with the maximum differences of S_{21} magnitude and S_{21} phase being 0.01 dB and 1 deg, respectively. Furthermore, the proposed model was found to be in excellent agreement with that of the high-frequency measurements with the maximum error for S_{21} magnitude and phase being approximately 0.05 dB and 2 deg below 20 GHz, respectively. The sensitivity studies indicate that the parasitic inductance, capacitance, resistance, and conductance have the first, second, third, and fourth most pronounced impacts on the *S*-parameters, respectively.

2) Taper Effect: The effect of via taper on the *RLCG* parameters was investigated. It was found that the parasitic capacitance and conductance values of tapered TPVs were 40% lower than those of straight ones. Also, the via taper increased the via resistance and inductance. The AC resistance was proven to be less influenced by the taper than the DC resistance, and the maximum inductance increase was about 80%.

3) Copper Plating: The effect of copper plating on the DC resistance of TPVs in glass was studied. The analysis showed that the fully-filled plating process resulted in lower via resistances than the conformal plating process, as expected, and the via taper helped reduce the minimum copper thickness required in the conformal plating to ensure

an adequate DC resistance close to that of the fully-filled plating. It is important to note that the current density is one of the key parameters to be considered in future work on TPVs in glass for high power applications.

4) Via Sidewall Roughness: The effect of via sidewall roughness on conductor loss was studied. Based on the observation of via sidewalls through SEM studies of TPVs formed by ArF excimer laser ablation, focused electrical-discharge method, and the Corning's drilling method, as well as the analysis through Hammerstad model, the following conclusions were drawn: 1) the surface roughness for ArF excimer laser ablation increased the conductor loss up to 16% at 20 GHz; 2) the surface roughness for focused electrical-discharge method did not have a significant impact up to 310 GHz; 3) the surface roughness for the Corning's drilling method remains negligible up to 1 THz.

5) Polymer Liner: The effect of polymer liners used as mechanical stress buffers to improve TPV reliability, was studied by a conformal mapping method, and the results showed that, as the thickness of the polymer liner increased to $1/4^{th}$ of the glass via diameter, the effective dielectric constant decreased by as much as 0.84, and as the pitch increased, the decreasing rate of the effective dielectric constant flattened out. Because the via capacitance decreases with the decreasing effective dielectric constant, resulting in larger impedance discontinuity, thick polymer liners are not electrically preferred for TPVs in glass, even though they improve the thermo-mechanical reliability of TPVs.

6) Nonlinear Taper: A computer-aided approach was proposed to analyze nonlinearly tapered TPVs drilled by TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method. Based on the observations through optical microscope or SEM, nonlinearly-tapered via shapes were approximated by the shape-preserving piecewise cubic interpolation, and the *RLCG* of such TPVs were computed and compared. The results showed that TPVs drilled by ArF laser, photo-sensitive method, and focused electrical discharge method had better performance than

those drilled by TiSa laser and CO_2 laser, but the performance differences were not that significant.

6.1.2 Design of Tapered TPVs for Signal Integrity

1) Signal Transition: The effect of via taper on signal transition was studied through *S*-parameters and eye diagrams. The results showed that via taper had negative impacts on the *S*-parameters, and as the aspect ratio increased, the effects were exacerbated. However, even for TPVs with the worst taper angles (75^o) at 100 GHz, the S_{21} magnitudes were still greater than -1 dB (90%). In addition, the eye-diagram analysis showed that unlike the noticeable eye-diagram degeneration for TSVs in silicon interposers, TPVs in glass interposers were almost electrically transparent. Even though the taper improves the eye diagrams of TSVs in silicon interposers, it does not have a significant impact for TPVs in glass interposers.

2) Impedance Discontinuity: The impedance discontinuity of TPVs in glass was analyzed through time-domain reflectometry (TDR), which is found to be inductive. The results showed that, as the taper angles decreased and the aspect ratios increased, the maximum impedance in the TDR response increased, exceeding the 5% design tolerance. Thus, two effective via configurations, namely GSG and four ground TPVs with a signal TPV (G4S1), were proposed to minimize this impedance discontinuity.

3) Crosstalk: The crosstalk was analyzed using GSG-to-GSG TPV test structures. An equivalent circuit model was developed for the analysis, which was verified against 3D EM simulations and measurements in the frequency domain. Based on the equivalent circuit model, it was found that both inductive and capacitive coupling coefficients decreased with decreasing taper angles and increasing aggressor-to-victim pitches. Two of the worst-case scenarios were studied. It can be concluded that reducing the pulse frequency to increase the rise and fall time and keeping the number of aggressor TPVs as low as possible are preferred approaches for crosstalk reduction. In addition, five

effective design techniques were proposed and investigated to suppress crosstalk noise. By comparing these techniques, it can be concluded that while GSG-GSG structures in a full Faraday cage provides the highest omni-directional isolation between aggressor and victim TPVs, it requires a large footprint and multiple ground TPVs. As a result, GSG-GSG with a grounded via fence is the preferred choice, as it achieves more than 30 dB isolation with compact size and minimum number of ground TPVs.

6.1.3 Millimeter-Wave Characterization of Tapered TPVs

Two methods, namely the short-circuit method and the ring-resonator method, were demonstrated for experimentally characterizing TPVs in glass up to millimeter-wave frequencies. The short-circuit method uses a one-port structure, with a TPV shorting the signal to the backside ground, generating a reflection to the incident signal, and the ring-resonator method uses a two-port structure, with TPVs inserted in the middle of a capacitively coupled ring structure to short the signal to the ground.

1) Method Analysis: An equivalent circuit was used for the short-circuit method to relate the *S*-parameters to the input impedance of TPVs, while an equivalent network based on the transmission-line model was used to analyze the ring-resonator method. Furthermore, the sensitivity of each method with respect to TPV resistance and inductance was investigated. The results showed that the short-circuit method was much less sensitive to via resistance than via inductance, and the ring-resonator method was only sensitive to via resistance and inductance at the specific resonant frequencies.

2) Experimental Characterization: Based on the two methods, glass substrate test vehicles were designed and fabricated by a novel low-cost panel-compatible process with high-aspect-ratio TPVs. Two sets of short-circuit test structures, as well as three ring resonators at 3 GHz, 6 GHz, and 9 GHz, were measured up to 50 GHz using a vector network analyzer (VNA) and on-wafer probes. Then, the TPV resistances and inductances were extracted from the measured *S*-parameters, and the measured values

closely matched those from 3D EM solver. For a 55-μm diameter TPV in a 366-μm-thick glass substrate, the measured resistance and inductance were ~1 Ω and 60 pH at 40 GHz, respectively.

3) Method Comparison: The short-circuit method and the ring-resonator method were compared in terms of accuracy and footprint. Compared to the short-circuit method, the accuracy achieved by the ring-resonator method is improved by about 1.60 times for via resistance and 1.03 times for via inductance. However, the footprint of the short-circuit test structures is 37 times smaller than that of the ring-resonator test structures.

6.1.4 Design Guidelines for Tapered TPVs

Based on the results presented in CHAPTERs 3 and 4, and the model-to-measurement correlations discussed in CHAPTER 5, the following set of comprehensive electrical design guidelines for tapered TPVs in glass interposers are presented in Table 6.1.

Table 6.1: Summary of design guidelines for tapered TPVs

	Design Guidelines
Resistance	• AR < 1.7, taper angle > 84.5^o • AR > 3.0, taper angle > 88^o
Inductance	• Maximum 80% increase • AR < 1.7, taper angle > 76^o • AR > 3.0, taper angle > 85^o
Capacitance and Conductance	• Maximum 40% decrease (not preferred)
Impedance	• Inductive discontinuity ≤ 10% • ≥ 2 ground TPVs
Crosstalk	• Inductive coupling decrease < 30% • Capacitive coupling decrease < 10% • NEXT < 10%, FEXT < 3% • ≥ 1 ground TPV for shielding

6.2 Key Contributions

The key contributions of this research are summarized below:

- A wideband scalable circuit model was proposed and verified for the first time to model tapered through-package vias (TPVs) in glass interposers.
- A novel computation method, that is to slice tapered TPVs into infinitesimally thin cylindrical pieces and to integrate them along TPVs, was developed with analytical and semi-analytical expressions derived for the via parasitics.
- The taper effects on via parasitics were fundamentally investigated, and the AC resistance was theoretically proven to be less influenced by taper than the DC resistance.
- The impacts of the TPV processes including copper plating, sidewall roughness, and polymer liner thickness on the electrical parameters were investigated for the first time.
- A novel computer-aided approach was proposed and developed to compute the parasitics of nonlinearly tapered TPVs drilled by TiSa laser, ArF laser, CO_2 laser, photo-sensitive method, and focused electrical discharge method.
- The signal transition through TPVs with various taper angles was studied in terms of frequency-domain *S*-parameters and time-domain eye diagrams. The results show that taper have a negative but insignificant impact on the TPV performance.
- The impedance discontinuity of TPVs was studied through time-domain reflectometry (TDR), showing an inductive discontinuity. Two design techniques were proposed to effectively minimize the impedance discontinuity.
- The crosstalk between TPVs was studied by an equivalent circuit model, and two of the worst-case scenarios were evaluated. Five design techniques were proposed and compared to effectively suppress the crosstalk.

- Two novel characterization methods, namely the short-circuit method and the ring-resonator method, were proposed and implemented to measure via parasitics.
- The sensitivity of each method with respect to via resistance and inductance was fundamentally derived.
- Based on the aforementioned two methods, test vehicles were designed and fabricated by a novel low-cost panel-compatible process with high-aspect-ratio TPVs.
- The two methods were compared in terms of the footprint and the accuracy.

6.3 Future Work

This dissertation explores the effect of via taper on the electrical parameters by electrical modeling, design and characterization for high-performance glass interposers. This research focused on computing and communications electronics. However, with glass proposed for new era of automotive electronics, there are other technical challenges that need to be addressed, and the following studies are proposed as future extensions of this research:

TPV Modeling

As the automotive electronics are exposed to high power and high temperature, a complex set of processes involving multiple physical phenomena takes place: the power is converted to heat; heat is manifested as temperature; temperature affects both electrical and mechanical performance, which might in turn affect power. Thus, TPVs in glass need to be modeled taking into account this electro-thermal-mechanical coupling, especially for the polymer liners. In addition, high power is often associated with large current. The precise current distribution in TPVs also has to be taken into account in TPV modeling.

TPV Design

If a single TPV is used to conduct a large current, electromigration might happen, decreasing the reliability of the system and causing the eventual loss of connections. Thus, one of the objectives for TPV design in high-power applications is to effectively distribute such a large current among many TPVs, probably by increasing the number of the TPVs and / or increasing the cross-sectional area of each TPV.

The autonomous driving electronics may require the packaging of both the digital and analog circuits into one substrate. While digital circuits are robust to noise, analog circuit, such as low-noise amplifiers, are very vulnerable to noise. The digital circuits generate noise resulting in the malfunction of the analog circuit. High digital-to-analog isolation may be necessary, which can be achieved by combining TPV designs with other techniques, such as electromagnetic band-gap structures.

The automotive radar system utilizes 77 GHz technologies. On one hand, TPVs and RDLs need to be designed to match to active circuits at this frequency with lowest insertion loss, while on the other hand, passive circuits, such as antenna arrays, matching networks, and power dividers can be designed and implemented with TPVs in glass.

TPV Characterization

Although the sidewall of TPVs in glass were qualitatively characterized by a scanning electron microscope (SEM) in this research, quantitative characterization, such as atomic-force microscopy (AFM), is necessary to provide more accurate details of the via sidewall roughness for conductor loss estimation. An electromigration test on TPVs and experimental characterization of TPVs at 77 GHz are also important.

The characterization of this dissertation mainly focuses on TPVs. However, microelectronic systems require the entire channel of signal transmission, including TPVs, RDLs and all interconnections. It is very important to study the signal integrity and power integrity of the entire channel in glass interposers.

6.4 Publications and Awards

This work results in the following peer-reviewed journals, conference proceeding, and awards.

6.4.1 Peer-Reviewed Journals

1. **J. Tong**, Y. Sato, K. Panayappan, V. Sundaram, A. F. Peterson, and R. R. Tummala, "Electrical Modeling and Analysis of Tapered Through-Package via in Glass Interposers," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, pp. 775-783, 2016.
2. **J. Tong**, Y. Sato, V. Sundaram, and R. R. Tummala, "Millimeter-Wave Modeling and Characterization of High-Aspect-Ratio Through-Package Vias in Glass Substrates," submitted to *IEEE Trans. Compon. Packa. Manuf. Technology*.. (Under Review)
3. **J. Tong**, V. Sundaram, and R. R. Tummala, "Electrical Analysis of Fabrication Process for Through-Package Vias in Glass Inteposers," to be submitted to *IEEE Trans. Electron Devices*.
4. **J. Tong**, K. Panayappan, V. Sundaram, and R. R. Tummala, "Signal Integrity Design and Analysis of Tapered Through-Package Vias in Glass Inteposers," to be submitted to *IEEE Trans. Compon. Packa. Manuf. Technol.*.
5. **J. Tong**, Y. Sato, V. Sundaram, and R. R. Tummala, "Resistance and Inductance Characterization of Through-Package Vias in Glass Substrates up to Millimeter-Wave Frequency," to be submitted to *IEEE Microw. Wireless Compon. Lett.*.
6. T. Huang, B. Chou, **J. Tong**, T. Ogawa, V. Sundaram, and R. R. Tummala, "Via-First Process to Enable Copper Metallization of Glass Interposers With High

Aspect Ration, Fine-Pitch Through-Package Vias," submitted to *IEEE Trans. Compon. Packag. Manuf. Technol.*. (Under Review)

6.4.2 Conference Proceedings

1. **J. Tong**, Y. Sato, S. Takahashi, N. Imajyo, A. F. Peterson, V. Sundaram, *et al.*, "High-frequency characterization of through package vias formed by focused electrical-discharge in thin glass interposers," in *Proc. IEEE 64th ECTC*, 2014, pp. 2271-2276.
2. **J. Tong**, V. Sundaram, A. Shorey, and R. Tummala, "Substrate-integrated waveguides in glass interposers with through-package-vias," in *Proc. IEEE 65th ECTC*, 2015, pp. 2222-2227.
3. **J. Tong**, K. Panayappan, V. Sundaram, and R. Tummala, "Electrical Comparison between TSV in Silicon and TPV in Glass for Interposer and Package Applications," in *Proc. IEEE 66th ECTC*, 2016 pp. 2581-2587.
4. V. Sundaram, **J. Tong**, K. Demir, T. Huang, A. Shorey, S. Pollard, *et al.*, "High Reliability and High Performance 30μm Through-Package-Vias in Ultra-Thin Bare Glass Interposer," in *International Symposium on Microelectronics*, 2014, pp. 000402-000408.
5. W. T. Khan, **J. Tong**, S. Sitaraman, V. Sundaram, R. Tummala, and J. Papapolymerou, "Characterization of electrical properties of glass and transmission lines on thin glass up to 50 GHz," in *Proc. IEEE 65th ECTC*, 2015, pp. 2138-2143.
6. K. Demir, A. Armutlulu, **J. Tong**, R. Pucha, V. Sundaram, and R. Tummala, "First demonstration of reliable copper-plated 30um diameter through-package-vias in ultra-thin bare glass interposers," in *Proc. IEEE 64th ECTC*, 2014, pp. 1098-1102.

6.4.3 Awards

1. First Place of Best Student Paper at 2015 Global Interposer Technology Workshop
2. Second Place of Best Student Paper at 2014 Global Interposer Technology Workshop

REFERENCES

[1] (2009, Dec.). *International Technology Roadmap for Semiconductors for Assembly & Packaging*. Available: http://www.itrs.net/home.html.

[2] Cisco. (2015, Jun.). *The Zettabyte Era: Trends and Analysis (Jun 23, 2015 ed.)*. Available: http://www.cisco.com/.

[3] T. S. Rappaport, S. Shu, R. Mayzus, Z. Hang, Y. Azar, K. Wang, *et al.*, "Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!," *IEEE Access*, vol. 1, pp. 335-349, 2013.

[4] R. Tummala, "System scaling: the next frontier for a new era of electronic systems," *Chip Scale Review*, vol. 19, pp. 5-8, Oct 2015.

[5] M. Santarini. (2011, Mar.). *Stacked and Loaded: Xilinx SSI, 28-Gbps I/O yield amazing FPGAs*. Available: http://www.eetimes.com/document.asp?doc_id=1278666.

[6] M. Maxfield. (2011, Oct.). *New Xilinx Virtex-7 2000T FPGA provides equivalent of 20 million ASIC gates*. Available: http://www.embedded.com/print/4230049.

[7] K. Heegon, C. Jonghyun, K. Myunghoi, K. Kiyeong, L. Junho, L. Hyungdong, *et al.*, "Measurement and Analysis of a High-Speed TSV Channel," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 2, pp. 1672-1685, 2012.

[8] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S. K. Lim, and R. Tummala, "Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications," in *Proc. IEEE 61st ECTC*, Lake Buena Vista, FL, USA, 2011, pp. 217-223.

[9] R. R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," *IEEE Trans. Adv. Packag.*, vol. 27, pp. 241-249, 2004.

[10] R. Tummala, *System on Package: Miniaturization of the Entire System*: McGraw-Hill Education, 2007.

[11] Corning. (2015, Jan.). *Product Information Sheet*. Available: https://www.corning.com/media/worldwide/csm/documents/Corning%20Semiconductor%20Glass%20Wafers%20PI%20Sheet_rev%2009022014.pdf.

[12] V. Sundaram, J. Tong, K. Demir, T. Huang, A. Shorey, S. Pollard, *et al.*, "High Reliability and High Performance 30μm Through-Package-Vias in Ultra-Thin Bare Glass Interposer," in *International Symposium on Microelectronics*, San Diego, CA, USA, 2014, pp. 000402-000408.

[13] A. Shorey, S. Pollard, A. Streltsov, G. Piech, and R. Wagner, "Development of substrates for through glass vias (TGV) for 3DS-IC integration," in *Proc. IEEE 62nd ECTC*, San Diego, CA, USA, 2012, pp. 289-291.

[14] A. Shorey, P. Cochet, A. Huffman, J. Keech, M. Lueck, S. Pollard, *et al.*, "Advancements in fabrication of glass interposers," in *Proc. IEEE 64th ECTC*, Orlando, FL, USA, 2014, pp. 20-25.

[15] V. Sukumaran, "Through-package-via hole formation, metallization and characterization for ultra-thin 3D glass interposer packages," Ph.D. dissertation, Electrical and Computer Engineering, Georgia Institute of Technology, 2014.

[16] G. Kumar, "Modeling, design, fabrication and characterization of power delivery networks and resonance suppression in double-sided 3-D glass interposer packages," Ph.D. dissertation, Electrical and Computer Engineering, Georgia Institute of Technology, 2015.

[17] T. Bandyopadhyay, "Modeling, design, and characterization of through vias in silicon and glass interposers," Ph.D. dissertation, Electrical and Computer Engineering, Georgia Institute of Technology, 2011.

[18] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of Microstrip Line on Si-SiO_2 System," *IEEE Trans. Microw. Theory Tech.*, vol. 19, pp. 869-881, 1971.

[19] I. Ndip, B. Curran, K. Lobbicke, S. Guttowski, H. Reichl, K. Lang, *et al.*, "High-Frequency Modeling of TSVs for 3-D Chip Integration and Silicon Interposers Considering Skin-Effect, Dielectric Quasi-TEM and Slow-Wave Modes," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, pp. 1627-1641, 2011.

[20] R. Beica, P. Siblerud, C. Sharbono, and M. Bernt, "Advanced Metallization for 3D Integration," in *Proc. 10th EPTC*, Singapore, 2008, pp. 212-218.

[21] F. Laermer and A. Schilp, "Method of anisotropically etching silicon," US5501893 A, 1996.

[22] N. Ranganathan, L. Da Yong, Y. Liu, L. Guo-Qiang, K. Prasad, and K. L. Pey, "Influence of Bosch Etch Process on Electrical Isolation of TSV Structures," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, pp. 1497-1507, 2011.

[23] K. Joohee, P. Jun So, C. Jonghyun, S. Eakhwan, C. Jeonghyeon, K. Heegon, *et al.*, "High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, pp. 181-195, 2011.

[24] L. Brusberg, H. Schroder, M. Topper, N. Arndt-Staufenbiel, J. Roder, M. Lutz, *et al.*, "Thin glass based packaging technologies for optoelectronic modules," in *Proc. 59th ECTC*, San Diego, CA, USA, 2009, pp. 207-212.

[25] S. Takahashi, K. Horiuchi, K. Tatsukoshi, M. Ono, N. Imajo, and T. Mobely, "Development of Through Glass Via (TGV) formation technology using electrical discharging for 2.5/3D integrated packaging," in *Proc. IEEE 63rd ECTC*, Las Vegas, NV, USA, 2013, pp. 348-352.

[26] L. Brusberg, M. Queisser, M. Neitz, H. Schr, x00F, der, *et al.*, "CO2-laser drilling of TGVs for glass interposer applications," in *Proc. IEEE 64th ECTC*, Orlando, FL, USA, 2014, pp. 1759-1764.

[27] R. Ostholt, N. Ambrosius, and R. A. Kruger, "High speed through glass via manufacturing technology for interposer," in *Proc. 2014 ESTC*, Helsinki, Finland, 2014, pp. 1-3.

[28] S. Takahashi, K. Tatsukoshi, M. Ono, and K. Kitaoka, "TGV technology for Glass interposer," in *Proc. 4th ESTC*, Amsterdam, Netherlands, 2012, pp. 1-3.

[29] L. Kuan-Chung, L. Yi-Chieh, H. Tzyy-Sheng, W. Sung-Mao, W. Chen-Chao, C. Chi-Tsung, *et al.*, "Vertical interconnect measurement techniques based on double-sided probing system and short-open-load-reciprocal calibration," in *Proc. IEEE 61st ECTC*, Lake Buena Vista, FL, USA, 2011, pp. 2130-2133.

[30] R. Chunghyun, C. Daehyun, L. Junho, L. Kwangyong, O. Taesung, and K. Joungho, "High frequency electrical circuit model of chip-to-chip vertical via interconnection for 3-D chip stacking package," in *Proc. IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging*, Austin, Texas, USA, 2005, pp. 151-154.

[31] R. Chunghyun, L. Jiwang, L. Hyein, L. Kwangyong, O. Taesung, and K. Joungho, "High Frequency Electrical Model of Through Wafer Via for 3-D Stacked Chip Packaging," in *Proc. 1st ESTC*, Dresden, Germany, 2006, pp. 215-220.

[32] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Trans. Electron Devices*, vol. 56, pp. 1873-1881, 2009.

[33] G. Katti, M. Stucchi, K. de Meyer, and W. Dehaene, "Electrical Modeling and Characterization of Through Silicon via for Three-Dimensional ICs," *IEEE Trans. Electron Devices*, vol. 57, pp. 256-262, 2010.

[34] X. Chuan, L. Hong, R. Suaya, and K. Banerjee, "Compact AC Modeling and Performance Analysis of Through-Silicon Vias in 3-D ICs," *IEEE Trans. Electron Devices*, vol. 57, pp. 3405-3417, 2010.

[35] T. Bandyopadhyay, H. Ki Jin, C. Daehyun, R. Chatterjee, M. Swaminathan, and R. Tummala, "Rigorous Electrical Modeling of Through Silicon Vias (TSVs) With MOS Capacitance Effects," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, pp. 893-903, 2011.

[36] H. Ki Jin, M. Swaminathan, and T. Bandyopadhyay, "Electromagnetic Modeling of Through-Silicon Via (TSV) Interconnections Using Cylindrical Modal Basis Functions," *IEEE Trans. Adv. Packag.*, vol. 33, pp. 804-817, 2010.

[37] L. En-Xiao, L. Er-Ping, E. Wei-Bin, L. Hui Min, L. Teck Guan, and G. Shan, "Compact Wideband Equivalent-Circuit Model for Electrical Modeling of Through-Silicon Via," *IEEE Trans. Microw. Theory Techn.*, vol. 59, pp. 1454-1460, 2011.

[38] C. Tai-Yu, W. Chuen-De, C. Yih-Peng, and W. Tzong-Lin, "A New Model for Through-Silicon Vias on 3-D IC Using Conformal Mapping Method," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, pp. 303-305, 2012.

[39] L. Yuanjun and L. Ye, "Closed-Form Expressions for the Resistance and the Inductance of Different Profiles of Through-Silicon Vias," *IEEE Electron Device Lett.*, vol. 32, pp. 393-395, 2011.

[40] X. Biancun and M. Swaminathan, "Electromagnetic modeling of non-uniform through-silicon via (TSV) interconnections," in *Proc. IEEE 16th Workshop on SPI*, Sorrento, Italy, 2012, pp. 43-46.

[41] L. Sheng, T. Wanchun, Z. Wei, W. Gui, and Y. L. Chow, "Capacitance and Conductance of Through Silicon Vias With Consideration of Multilayer Media and Different Shapes," *IEEE Trans. Compon. Packag. Manuf. Technol.,* vol. 5, pp. 256-264, 2015.

[42] K. Cheolbok and Y. Yong-Kyu, "High frequency characterization and analytical modeling of through glass via (TGV) for 3D thin-film interposer and MEMS packaging," in *Proc. IEEE 63rd ECTC*, Las Vegas, NV, USA, 2013, pp. 1385-1391.

[43] K. Jihye, H. Insu, K. Youngwoo, C. Jonghyun, V. Sundaram, R. Tummala, *et al.*, "Precise RLGC modeling and analysis of through glass via (TGV) for 2.5D/3D IC," in *Proc. IEEE 65th ECTC*, San Diego, CA, USA, 2015, pp. 254-259.

[44] X. Zheng, A. Beece, Z. Dingyou, C. Qianwen, C. Kuan-Neng, K. Rose, *et al.*, "Crosstalk evaluation, suppression and modeling in 3D through-strata-via (TSV) network," in *Proc. IEEE Int. 3D IC*, Munich, Germany, 2010, pp. 1-8.

[45] X. Zheng and L. Jian-Qiang, "High-Speed Design and Broadband Modeling of Through-Strata-Vias (TSVs) in 3D Integration," *IEEE Trans. Compon. Packag. Manuf. Technol.,* vol. 1, pp. 154-162, 2011.

[46] X. Zheng and L. Jian-Qiang, "Three-Dimensional Coaxial Through-Silicon-Via (TSV) Design," *IEEE Electron Device Lett.,* vol. 33, pp. 1441-1443, 2012.

[47] C. Jonghyun, S. Eakhwan, Y. Kihyun, P. Jun So, K. Joohee, L. Woojin, *et al.*, "Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," *IEEE Trans. Compon. Packag. Manuf. Technol.,* vol. 1, pp. 220-233, 2011.

[48] C. Chun-Hsien, Y. Hsun, L. Ching-Kuan, L. Yu-Min, C. Ren-Shin, Z. Chau-Jie, *et al.*, "Performance and process characteristic of glass interposer with through-glass-via(TGV)," in *Proc. IEEE Int. 3D Syst. Integr. Conf.*, San Francisco, CA, USA, 2013, pp. 1-7.

[49] I. Hwang, J. Kim, Y. Kim, J. Cho, J. Kim, V. Sundaram, *et al.*, "Analysis of through glass via (TGV) noise coupling effect to noise figure of 2.4GHz LNA on glass interposer," in *Proc. IEEE EDAPS*, Seoul, Korea, 2015, pp. 85-88.

[50] H. Insu, J. Kim, K. Youngwoo, C. Jonghyun, and J. Kim, "Noise coupling modeling and analysis of through glass via(TGV)," in *Proc. Int. 3D Syst. Integr. Conf.*, Sendai, Japan, 2015, pp. TS8.34.1-TS8.34.5.

[51] J. Dong Min, R. Chunghyun, L. Kwang Yong, C. Byeong Hoon, K. Joungho, O. Tae Sung, *et al.*, "Development and Evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV)," in *Proc. 57th ECTC*, Reno, NV, USA, 2007, pp. 847-852.

[52] Y. P. R. Lamy, K. B. Jinesh, F. Roozeboom, D. J. Gravesteijn, and W. F. A. Besling, "RF Characterization and Analytical Modelling of Through Silicon Vias and Coplanar Waveguides for 3D Integration," *IEEE Trans. Adv. Packag.*, vol. 33, pp. 1072-1079, 2010.

[53] M. Sunohara, H. Sakaguchi, A. Takano, R. Arai, K. Murayama, and M. Higashi, "Studies on electrical performance and thermal stress of a silicon interposer with TSVs," in *Proc. 60th ECTC*, Las Vegas, NV, USA, 2010, pp. 1088-1093.

[54] Q. Chen, T. Bandyopadhyay, Y. Suzuki, L. Fuhan, V. Sundaram, R. Pucha, *et al.*, "Design and demonstration of low cost, panel-based polycrystalline silicon interposer with through-package-vias (TPVs)," in *Proc. IEEE 61st ECTC*, Lake Buena Vista, FL, USA, 2011, pp. 855-860.

[55] J. H. Wu, J. Scholvin, and J. A. del Alamo, "An insulator-lined silicon substrate-via technology with high aspect ratio," *IEEE Trans. Electron Devices*, vol. 48, pp. 2181-2183, 2001.

[56] L. L. W. Leung and K. J. Chen, "Microwave Characterization and Modeling of High Aspect Ratio Through-Wafer Interconnect Vias in Silicon Substrates," *IEEE Trans. Microw. Theory Techn.*, vol. 53, pp. 2472-2480, 2005.

[57] J. Y. Lee, S. K. Lee, and J. H. Park, "Fabrication of void-free copper filled through-glass-via for wafer-level RF MEMS packaging," *Electronics Letters*, vol. 48, pp. 1076-1077, 2012.

[58] M. Topper, M. Wohrman, L. Brusberg, N. Jurgensen, I. Ndip, and K. D. Lang, "Development of a high density glass interposer based on wafer level packaging technologies," in *Proc. IEEE 64th ECTC*, Orlando, FL, USA, 2014, pp. 1498-1503.

[59] S. Kuramochi, S. Koiwa, T. Takano, M. Akazawa, H. Mawatari, K. Suzuki, *et al.*, "Advanced interposers with metalized through via," in *Proc. EMPC*, Friedrichshafen, Germany, 2015, pp. 1-6.

[60] S. H. Hall and H. L. Heck, *Advanced signal integrity for high-speed digital designs*: John Wiley & Sons, 2011.

[61] E. Bogatin, *Signal Integrity - Simplified*, 2nd ed.: Prentice Hall Professional Technical Reference, 2010.

[62] D. M. Pozar, *Microwave Engineering*, 4th ed.: Wiley, 2011.

[63] F. E. Terman, *Radio engineer's handbook*: McGraw-Hill Book Company, inc., 1943.

[64] Atotech. (2016, Jul.). *A Novel Approach in HDI Microvia Manufacturing: Understanding Laser Direct Drilling*. Available: http://www.atotech.com/fileadmin/pdf/papers/el/A_Novel_Approach_in_HDI_Microvia_Manufacturing.pdf.

[65] Corning. (2015, Jun.). *Corning EAGLE XG Slim GLass Substrates*. Available: https://www.corning.com/worldwide/en/products/display-glass/products/eagle-xg-slim.html.

[66] A. B. Shorey and R. Lu, "Progress and application of through glass via (TGV) technology," in *Proc. Pan Pacific Microelectronics Symposium*, 2016, pp. 1-6.

[67] ANSYS Inc. ANSYS HFSS Software [Online]. Available: http://www.ansys.com/Products/Simulation+Technology/Electronics/Signal+Integrity/ANSYS+HFSS.

[68] L. Yang and Z. Huiyan, "Shape preserving piecewise cubic interpolation," *Applied Mathematics*, vol. 11, pp. 419-424, 1996.

[69] K.-C. Lu and T.-S. Horng, "Comparative modeling of single-ended through-silicon vias in GS and GSG configurations up to v-band frequencies," *Progress In Electromagnetics Research*, vol. 143, pp. 559-574, 2013.

[70] C. Erli and S. Y. Chou, "Characteristics of coplanar transmission lines on multilayer substrates: modeling and experiments," *IEEE Trans. Microw. Theory Techn.*, vol. 45, pp. 939-945, 1997.

[71] M. Kirschning, R. H. Jansen, and N. H. L. Koster, "Measurement and Computer-Aided Modeling of Microstrip Discontinuities by an Improved Resonator Method," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, 1983, pp. 495-497.

[72] H. Lung-Hwa and C. Kai, "Equivalent lumped elements G, L, C, and unloaded Q's of closed- and open-loop ring resonators," *IEEE Trans. Microw. Theory Techn.*, vol. 50, pp. 453-460, 2002.

VITA

JIALING TONG

TONG was born in Longyan, Fujian, China. He received the B.S. degree in information engineering from Southeast University, Nanjing, Jiangsu, China, in 2009 and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2015, where he is pursuing the Ph.D. degree with the 3-D Systems Packaging Research Center.

From 2009 to 2012, he was a Graduate Research Assistant with the Center for Microwave and RF Technologies, Shanghai Jiao Tong University, Shanghai, China. His research interest includes electrical modeling, design and characterization of through-package-vias in silicon and glass interposers, electromagnetic simulation, signal and power integrity analysis, and mm-wave characterization.

Mr. Tong was a recipient of the Best Student Paper Award (1st place) at 2015 Global Interposer Technology Workshop, Bosch Scholarship in 2011, and RIM (Research In Motion) Scholarship in 2010.